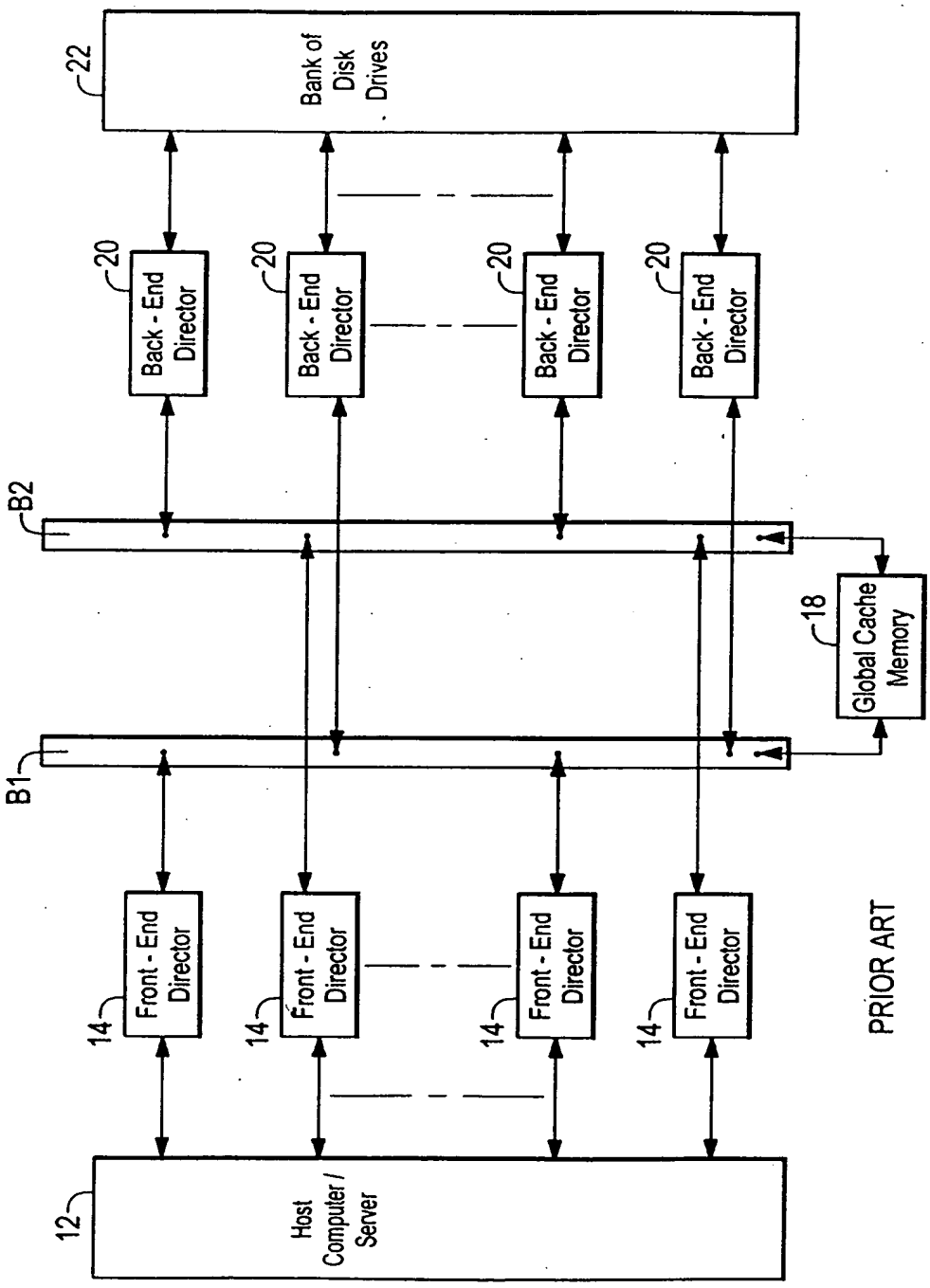


PRIOR ART

FIG. 1

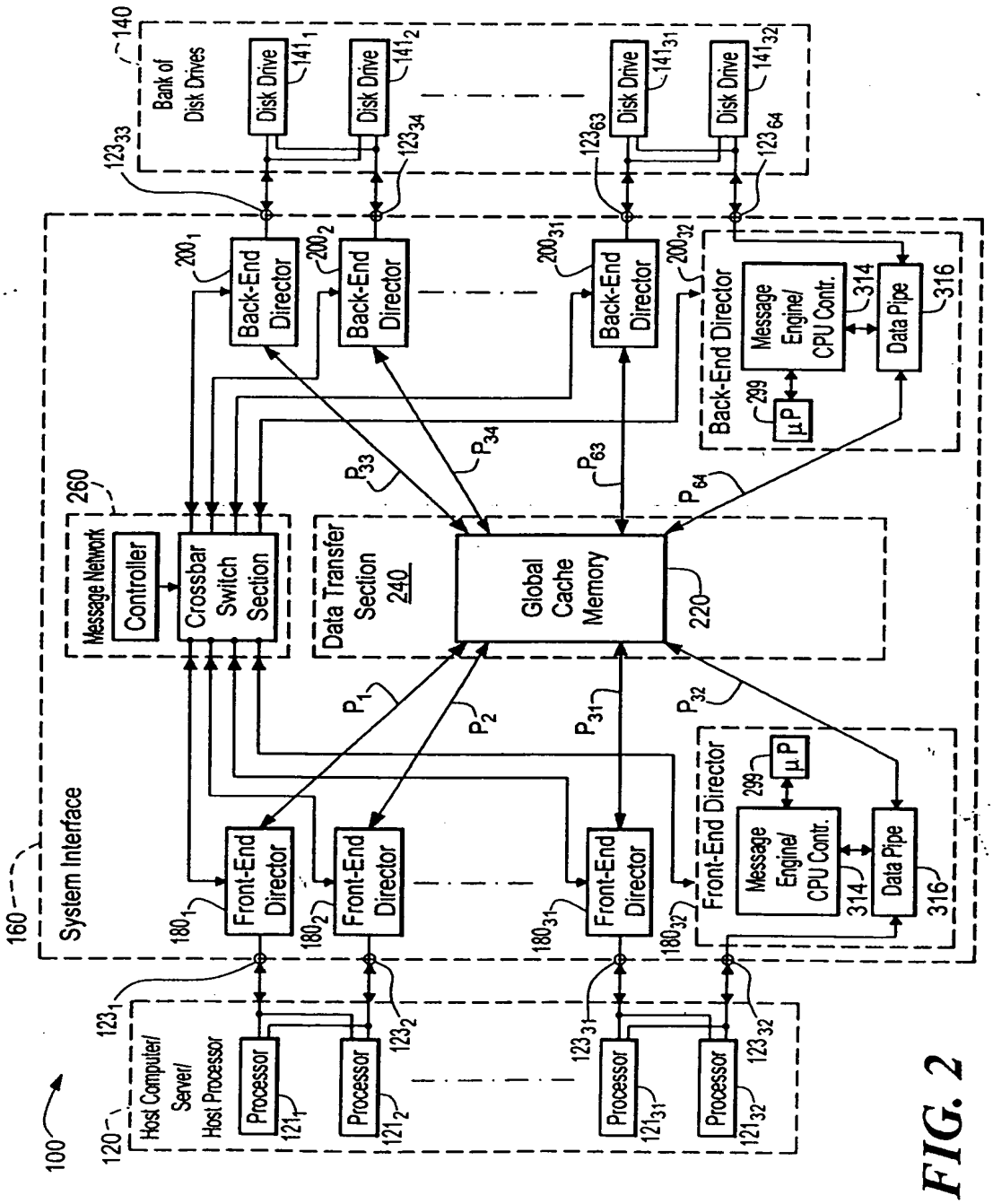

100
120
Host Computer/ Server/ Host Processor
Processor
121
123
160
System Interface
180
Front-End Director
Front-End Director
Front-End Director
Front-End Director
Message Engine/ CPU Contr.
314
Data Pipe
316
299
μP
Message Network
Controller
Crossbar Switch Section
260
Data Transfer Section 240
Global Cache Memory
220
P1
P2
P31
P32
P33
P34
P63
P64
200
Back-End Director
Back-End Director
Back-End Director
Back-End Director
Message Engine/ CPU Contr.
314
Data Pipe
316
299
μP
140
Bank of Disk Drives
Disk Drive
141

FIG. 2

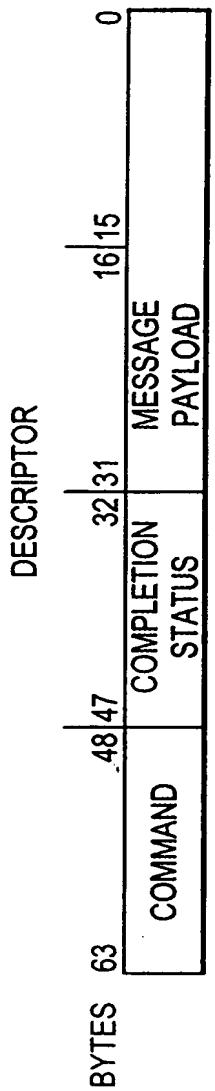

DESCRIPTOR
BYTES
63
48
47
32
31
16
15
0
COMMAND
COMPLETION STATUS
MESSAGE PAYLOAD

FIG. 2A

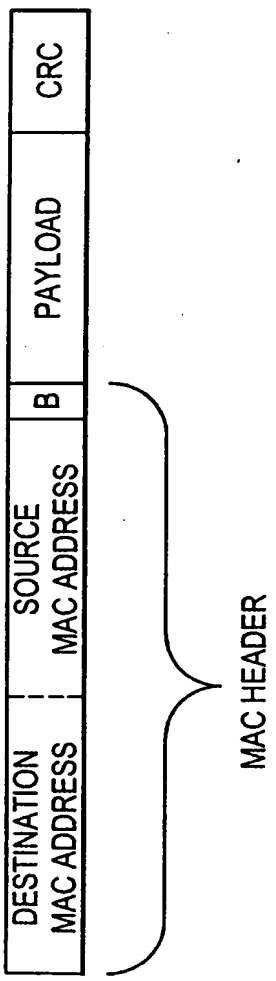

MAC PACKET
DESTINATION MAC ADDRESS
SOURCE MAC ADDRESS
B
PAYLOAD
CRC
MAC HEADER

FIG. 2B

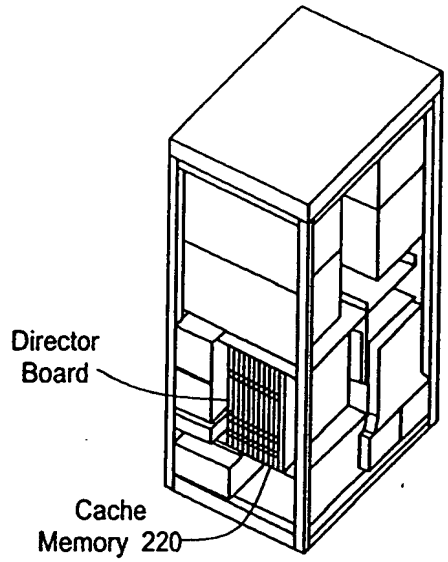

Director
Board
Cache
Memory 220

FIG. 3

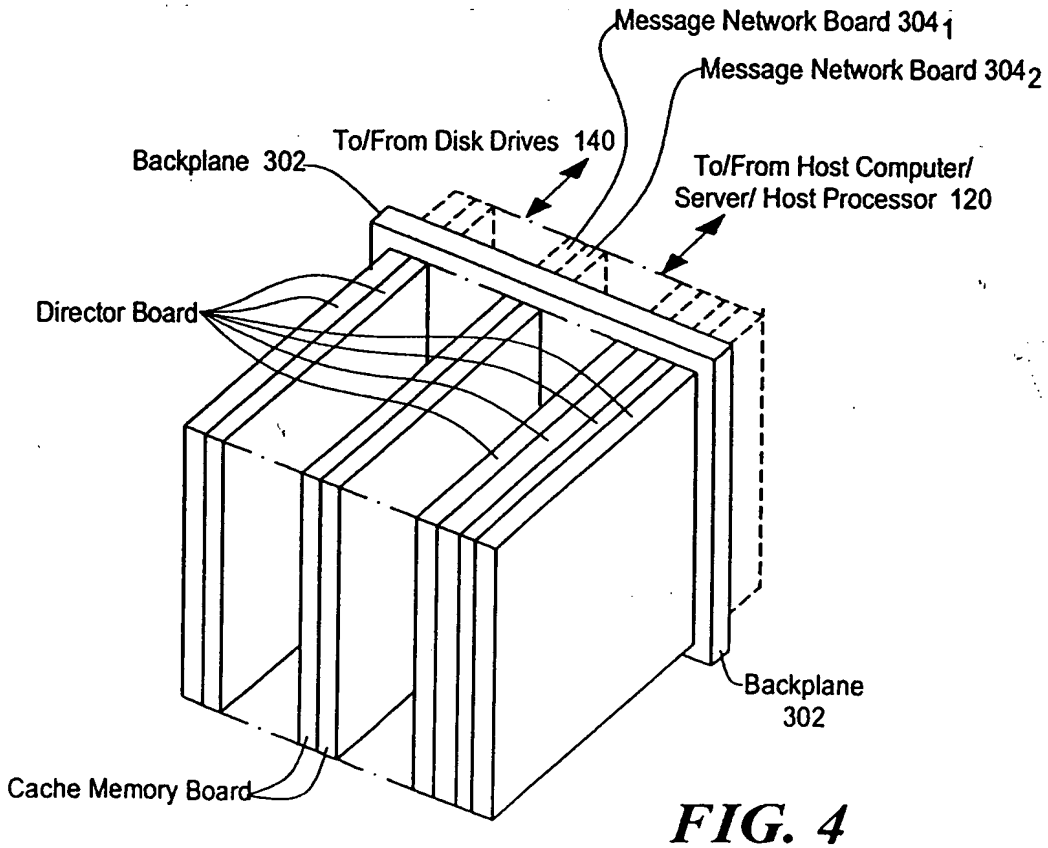
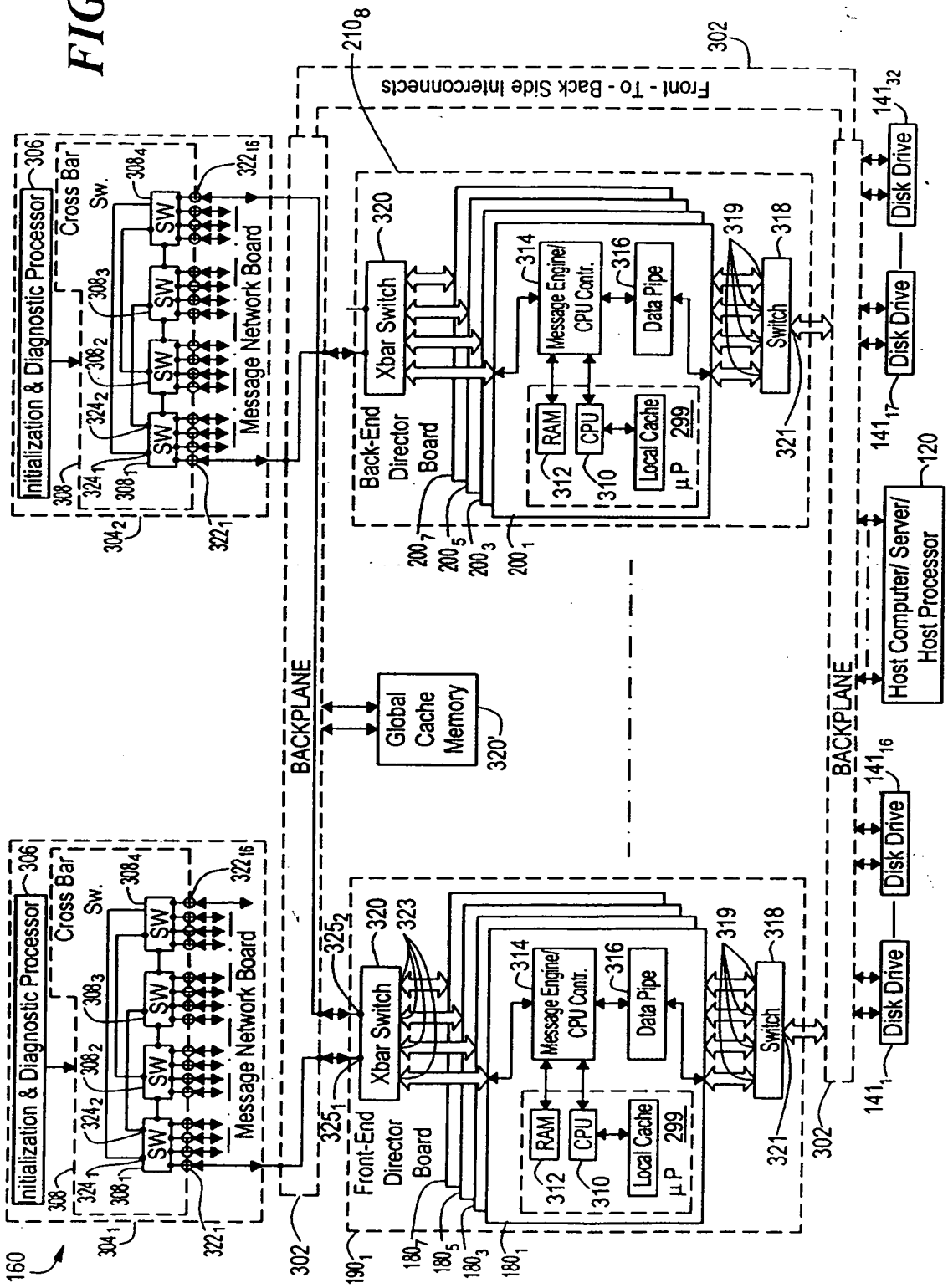

Message Network Board 304 1
Message Network Board 304 2
To/From Disk Drives 140
Backplane 302
To/From Host Computer/
Server/ Host Processor 120
Director Board
Backplane
302
Cache Memory Board

FIG. 4

FIG. 5


160
Initialization & Diagnostic Processor
306
Cross Bar Sw.
SW
Message Network Board
BACKPLANE
Front - To - Back Side Interconnects
Back-End Director Board
Front-End Director Board
Xbar Switch
Message Engine/ CPU Contr.
Data Pipe
Switch
RAM
CPU
Local Cache
µP 299
Global Cache Memory
Host Computer/ Server/ Host Processor
Disk Drive

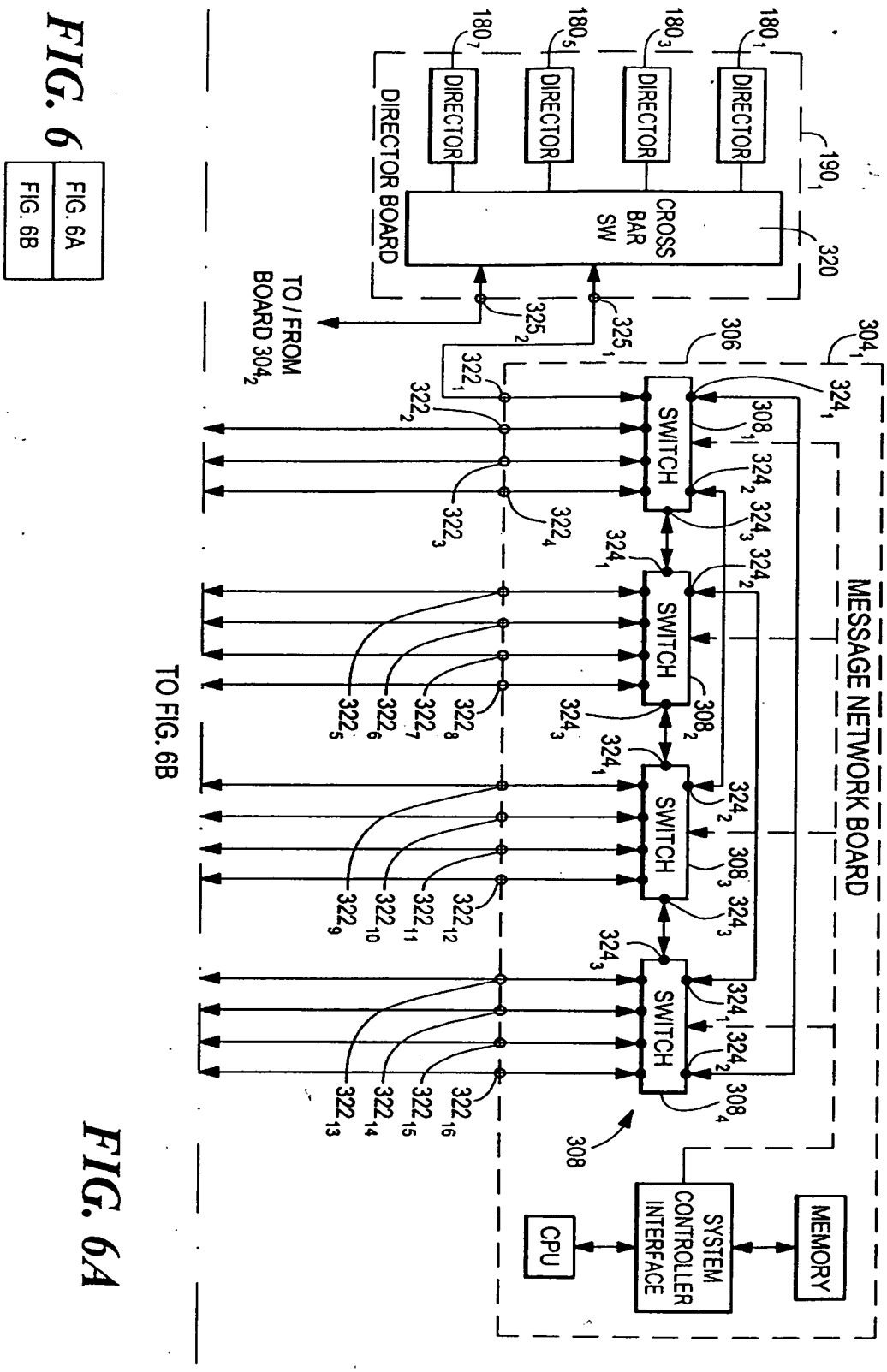


FIG. 6A

FIG. 6

FIG. 6A
FIG. 6B

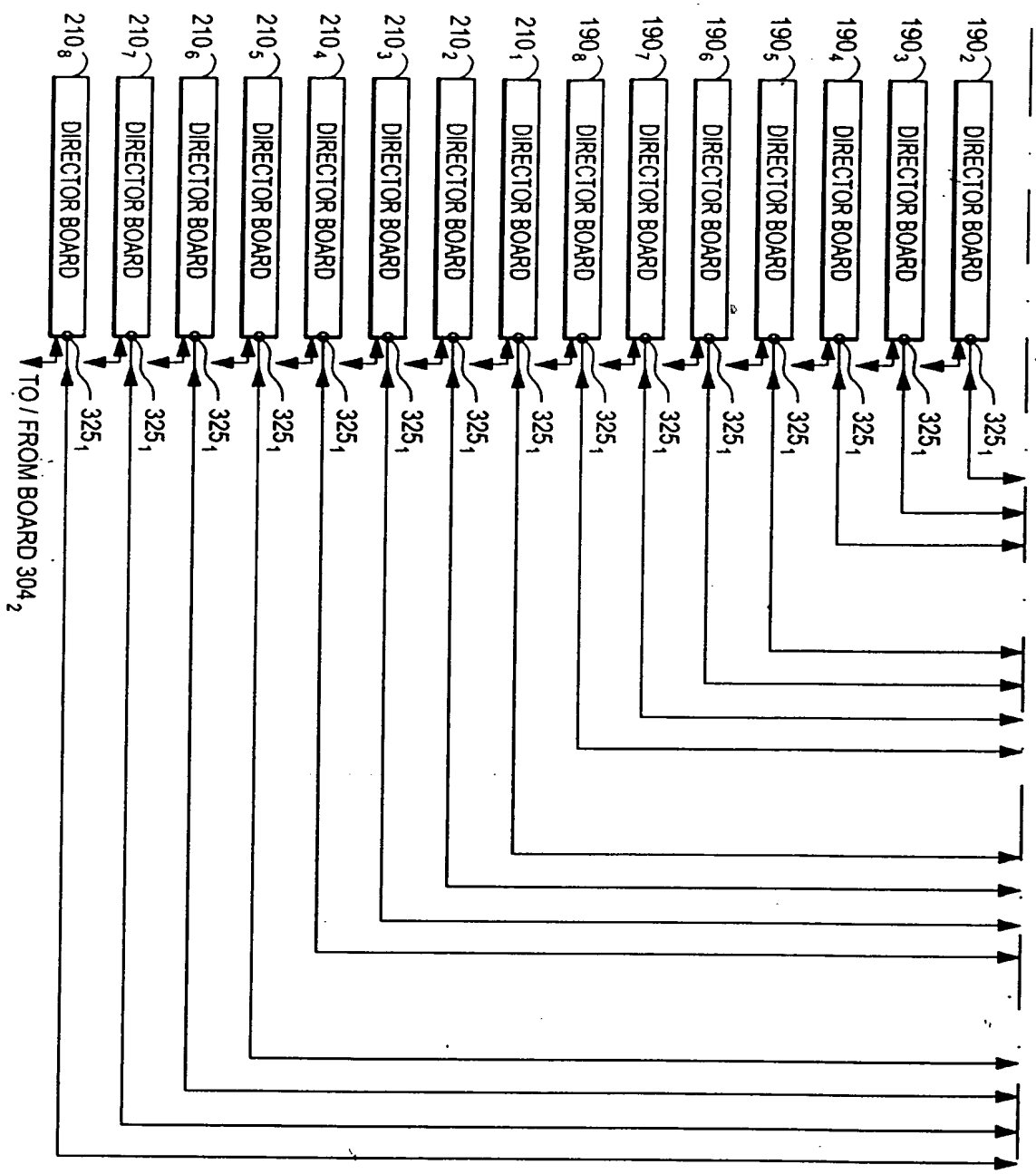

190_2 DIRECTOR BOARD
190_3 DIRECTOR BOARD
190_4 DIRECTOR BOARD
190_5 DIRECTOR BOARD
190_6 DIRECTOR BOARD
190_7 DIRECTOR BOARD
190_8 DIRECTOR BOARD
210_1 DIRECTOR BOARD
210_2 DIRECTOR BOARD
210_3 DIRECTOR BOARD
210_4 DIRECTOR BOARD
210_5 DIRECTOR BOARD
210_6 DIRECTOR BOARD
210_7 DIRECTOR BOARD
210_8 DIRECTOR BOARD
325_1
FROM FIG. 6A
TO / FROM BOARD 304_2

FIG. 6B

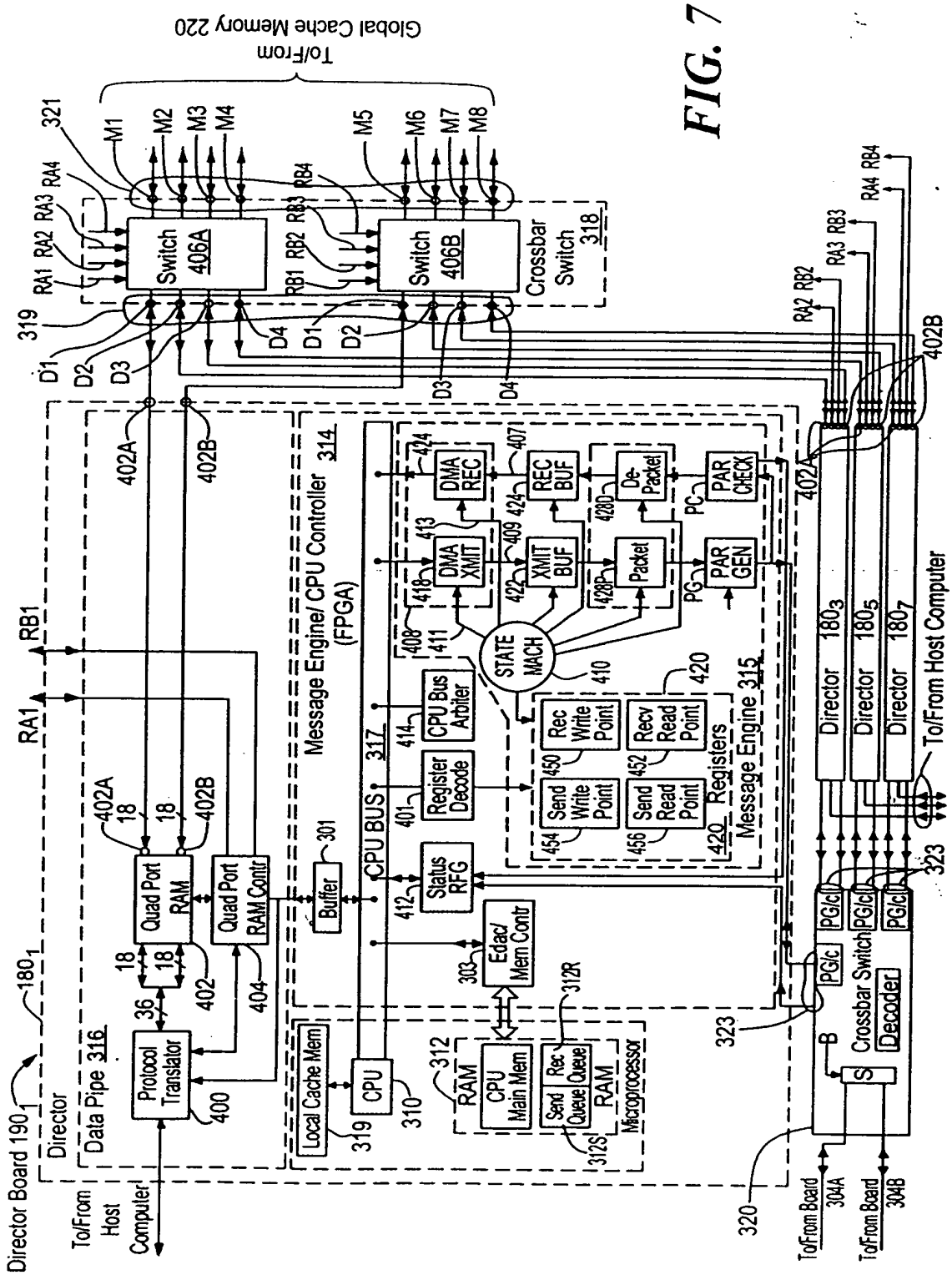

To/From Global Cache Memory 220
Switch 406A
Switch 406B
Crossbar Switch 318
Director Board 190
Director
Data Pipe 316
Protocol Translator
Quad Port RAM
Quad Port RAM Contr
Buffer
Message Engine/ CPU Controller 314
(FPGA)
CPU BUS 317
CPU Bus Arbiter
Register Decode
Status RFG
Edac/ Mem Contr
Local Cache Mem
CPU
CPU Main Mem
Send Queue
Rec Queue
RAM
Microprocessor
DMA REC
REC BUF
De-Packet
PAR CHECK
DMA XMIT
XMIT BUF
Packet
PAR GEN
STATE MACH
Rec Write Point
Recv Read Point
Send Write Point
Send Read Point
Message Engine 315
Registers
Director 180₃
Director 180₅
Director 180₇
To/From Host Computer
Crossbar Switch
Decoder
PG/c
To/From Host Computer
To/From Board 304A
To/From Board 304B

FIG. 7

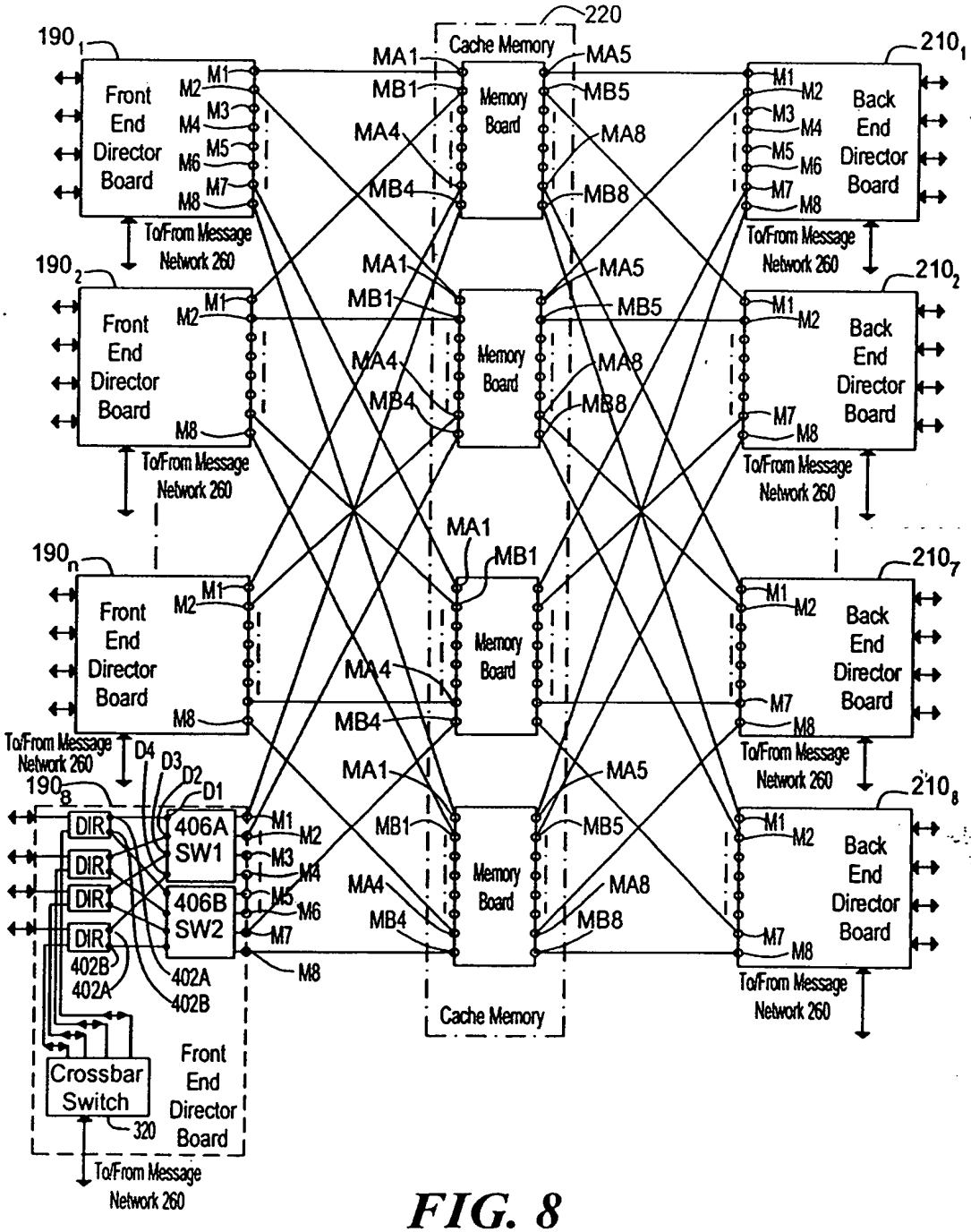

220
Cache Memory
190 1
Front End Director Board
M1 M2 M3 M4 M5 M6 M7 M8
To/From Message Network 260
190 2
190 n
190 8
DIR
406A SW1
406B SW2
D4 D3 D2 D1
402B 402A
402A 402B
Crossbar Switch
320
Front End Director Board
MA1 MB1 MA4 MB4 MA5 MB5 MA8 MB8
Memory Board
210 1
210 2
210 7
210 8
Back End Director Board
Cache Memory

FIG. 8

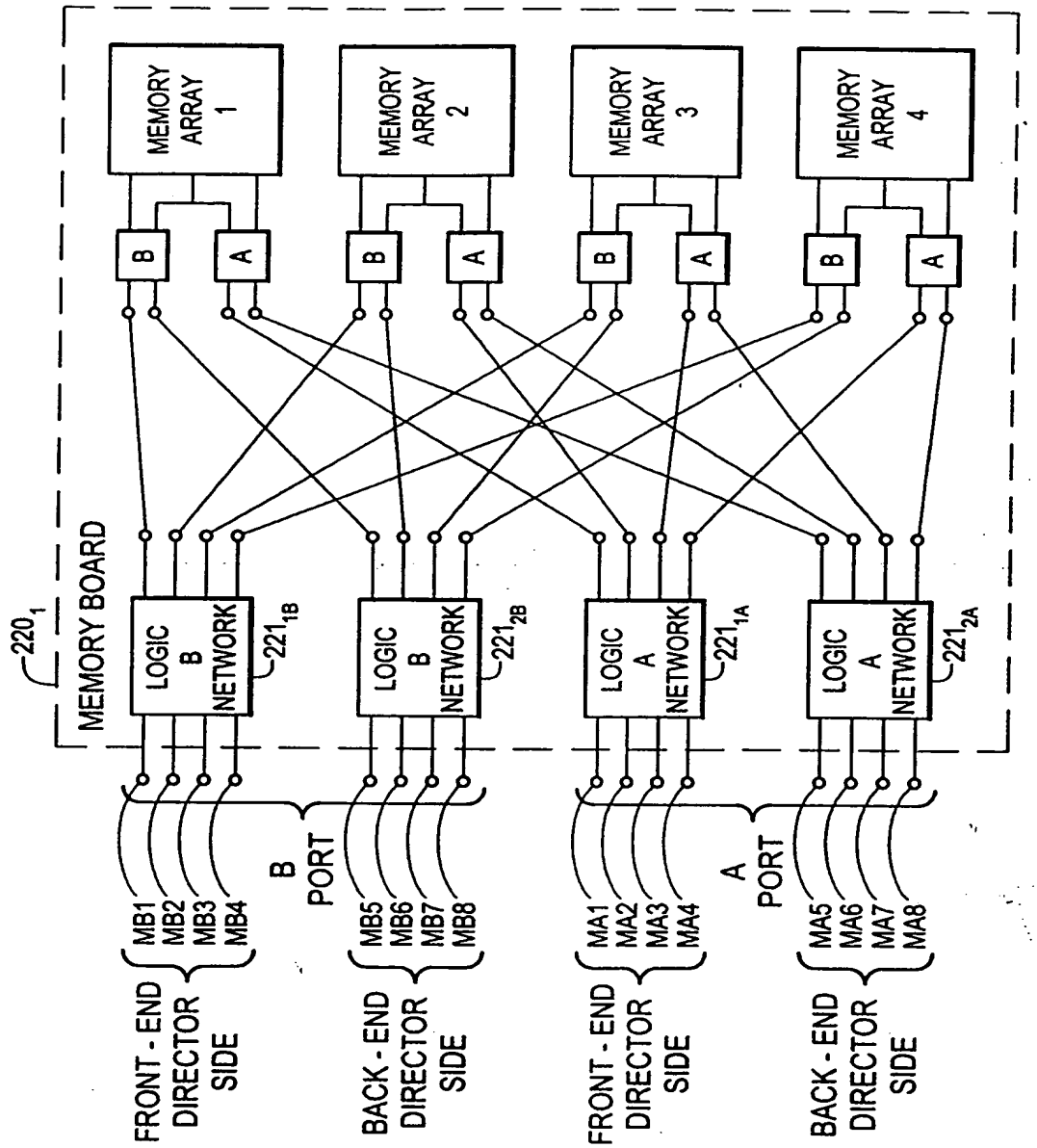

MEMORY BOARD
220 1
MEMORY ARRAY 1
MEMORY ARRAY 2
MEMORY ARRAY 3
MEMORY ARRAY 4
B
A
LOGIC B NETWORK
221 1B
LOGIC B NETWORK
221 2B
LOGIC A NETWORK
221 1A
LOGIC A NETWORK
221 2A
B PORT
A PORT
MB1
MB2
MB3
MB4
MB5
MB6
MB7
MB8
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
FRONT - END DIRECTOR SIDE
BACK - END DIRECTOR SIDE
FRONT - END DIRECTOR SIDE
BACK - END DIRECTOR SIDE

FIG. 8A

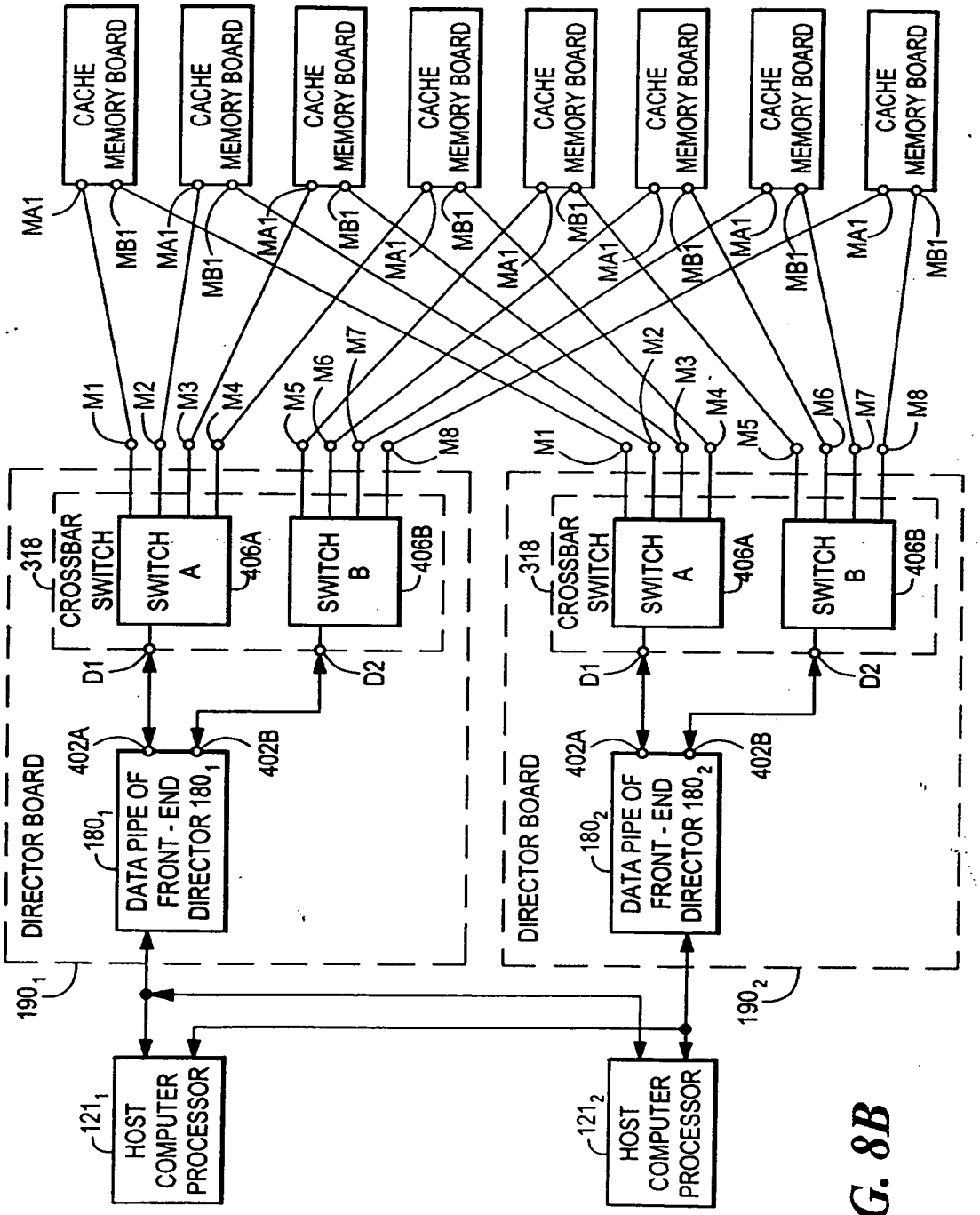

CACHE MEMORY BOARD
MA1
MB1
M1
M2
M3
M4
M5
M6
M7
M8
CROSSBAR SWITCH
318
SWITCH A
406A
SWITCH B
406B
D1
D2
DIRECTOR BOARD
402A
402B
DATA PIPE OF FRONT - END DIRECTOR 180$_1$
DATA PIPE OF FRONT - END DIRECTOR 180$_2$
180$_1$
180$_2$
190$_1$
190$_2$
HOST COMPUTER PROCESSOR
121$_1$
121$_2$

FIG. 8B

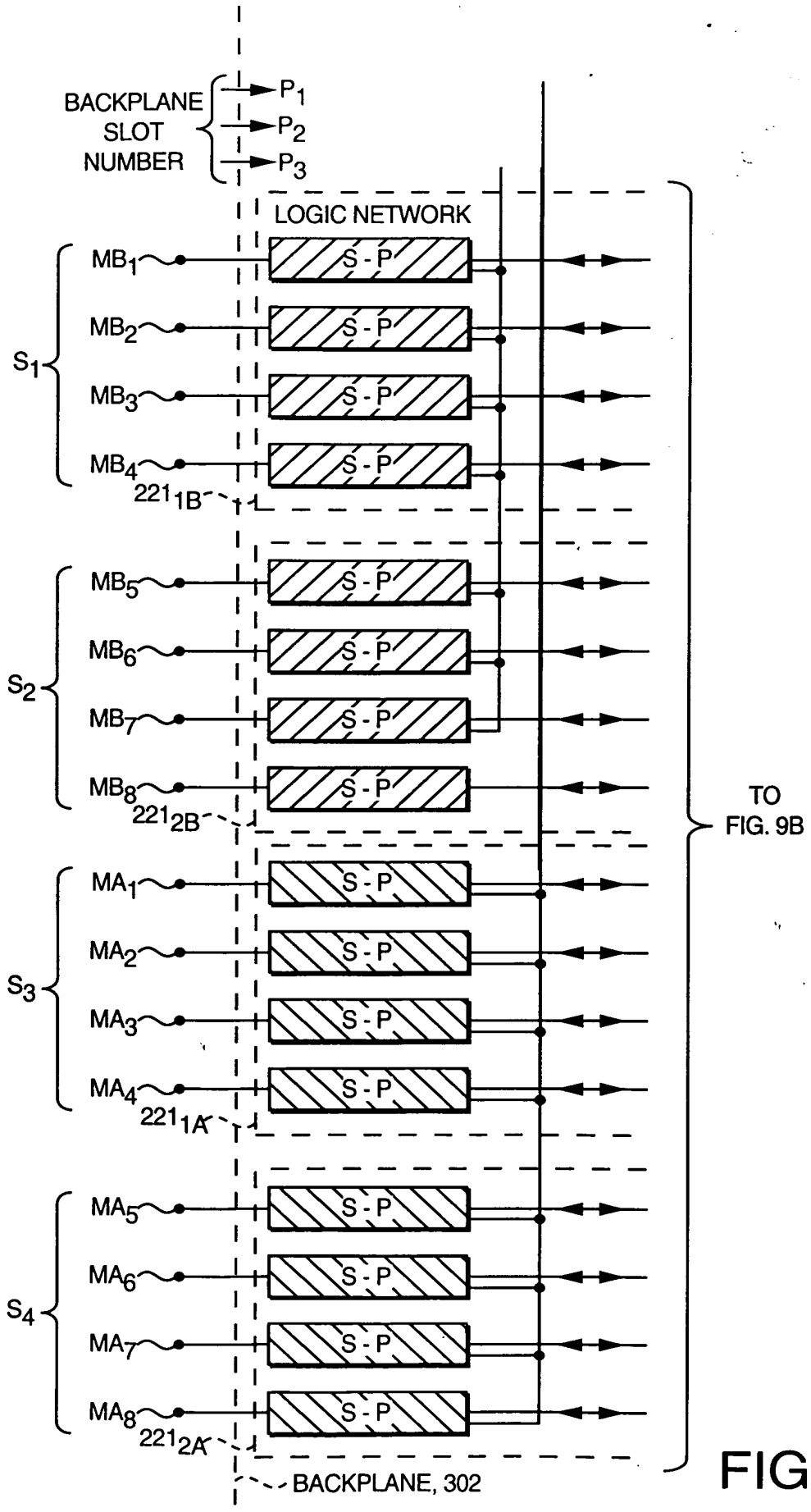
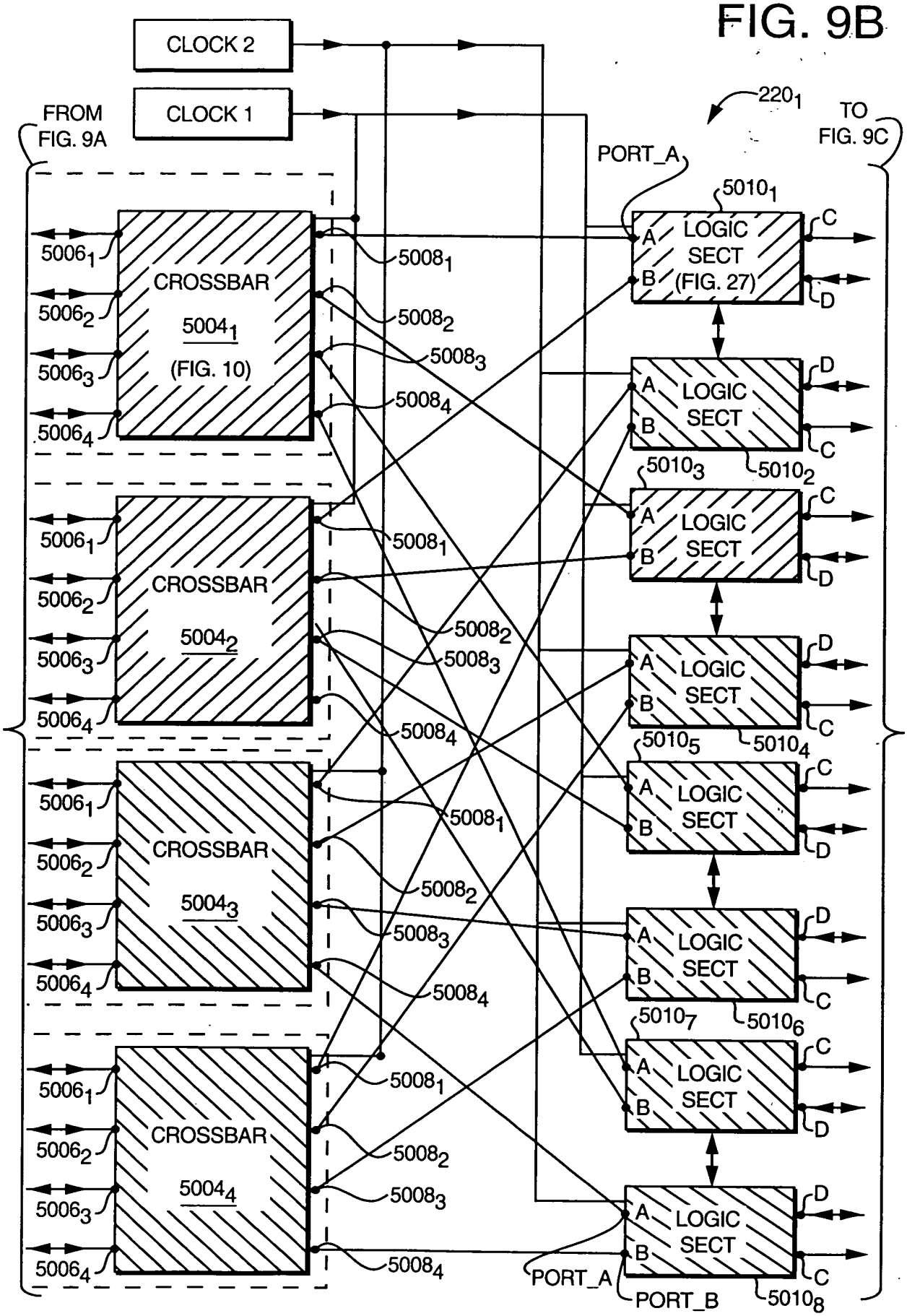

BACKPLANE SLOT NUMBER
P1
P2
P3
LOGIC NETWORK
S - P
MB1
MB2
MB3
MB4
MB5
MB6
MB7
MB8
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
S1
S2
S3
S4
221 1B
221 2B
221 1A
221 2A
TO FIG. 9B
BACKPLANE, 302

FIG. 9A

FIG. 9B


CLOCK 2
CLOCK 1
FROM FIG. 9A
TO FIG. 9C
220_1
PORT_A
5010_1
LOGIC SECT (FIG. 27)
5010_2
5010_3
5010_4
5010_5
5010_6
5010_7
5010_8
PORT_B
CROSSBAR 5004_1 (FIG. 10)
CROSSBAR 5004_2
CROSSBAR 5004_3
CROSSBAR 5004_4
5006_1
5006_2
5006_3
5006_4
5008_1
5008_2
5008_3
5008_4
A
B
C
D

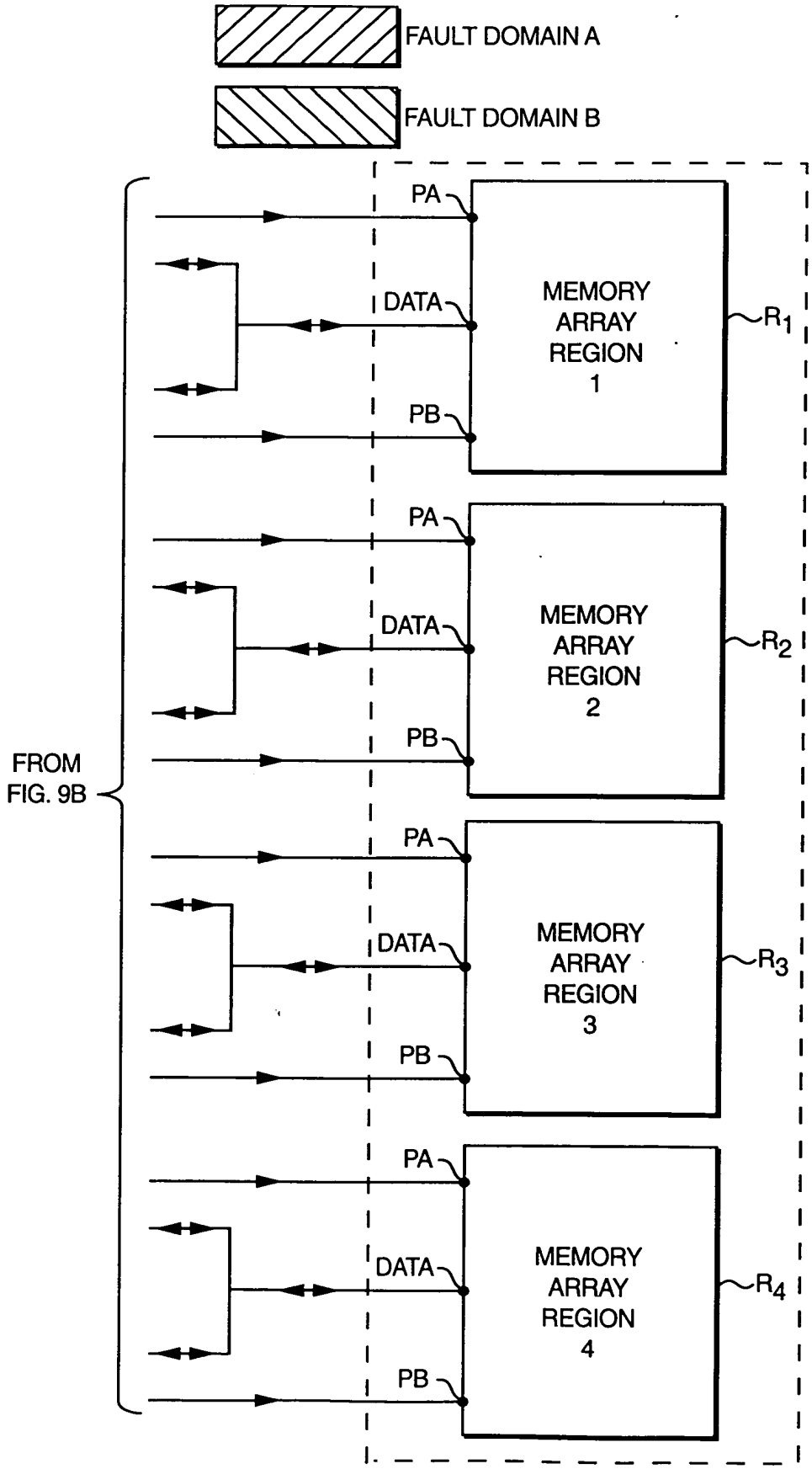
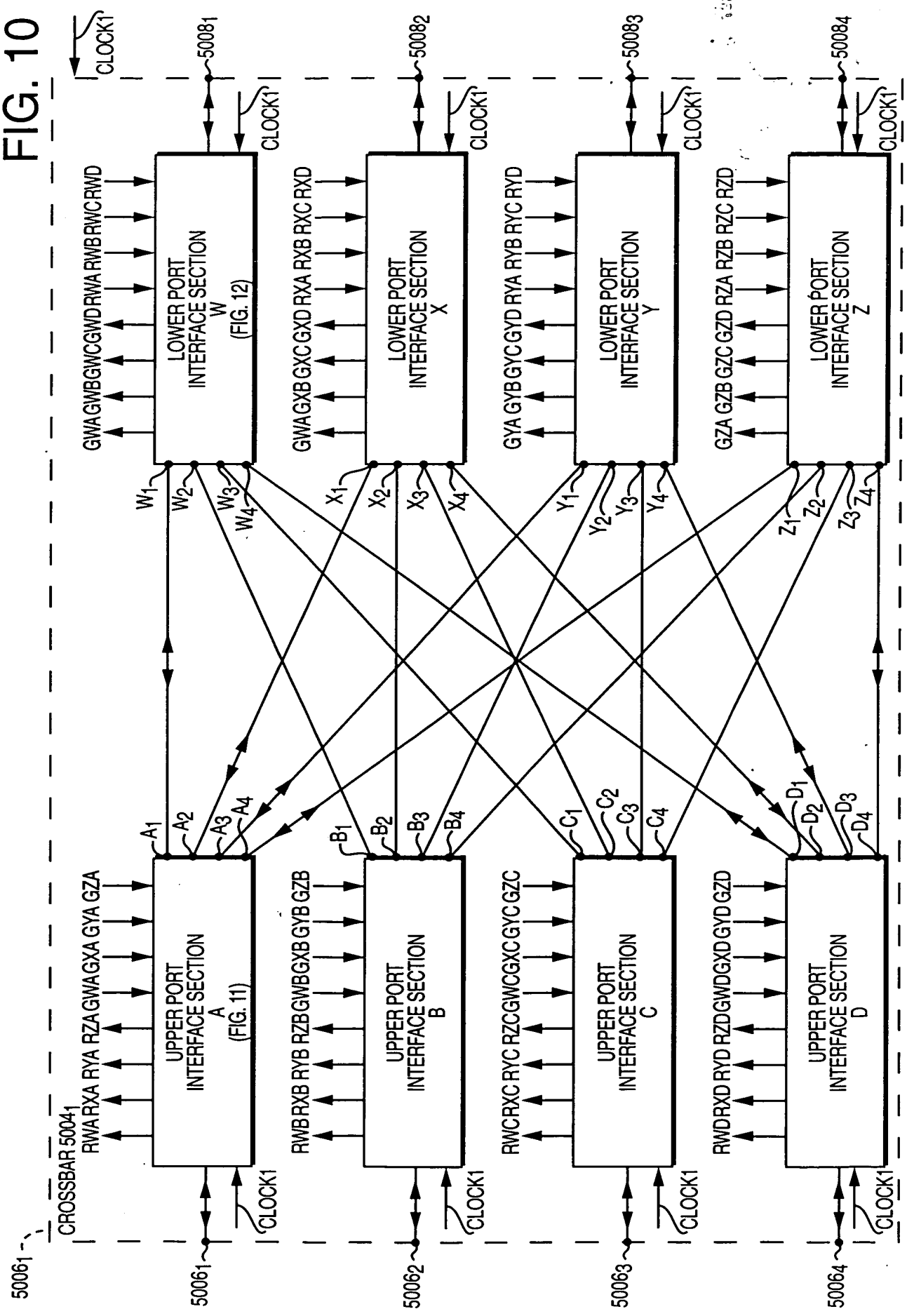

FAULT DOMAIN A
FAULT DOMAIN B
FROM FIG. 9B
PA
DATA
PB
MEMORY ARRAY REGION 1
R1
MEMORY ARRAY REGION 2
R2
MEMORY ARRAY REGION 3
R3
MEMORY ARRAY REGION 4
R4

FIG. 9C

FIG. 10


CLOCK1
50081
50082
50083
50084
LOWER PORT INTERFACE SECTION W (FIG. 12)
LOWER PORT INTERFACE SECTION X
LOWER PORT INTERFACE SECTION Y
LOWER PORT INTERFACE SECTION Z
GWA GWB GWC GWD RWA RWB RWC RWD
GXA GXB GXC GXD RXA RXB RXC RXD
GYA GYB GYC GYD RYA RYB RYC RYD
GZA GZB GZC GZD RZA RZB RZC RZD
W1 W2 W3 W4
X1 X2 X3 X4
Y1 Y2 Y3 Y4
Z1 Z2 Z3 Z4
A1 A2 A3 A4
B1 B2 B3 B4
C1 C2 C3 C4
D1 D2 D3 D4
UPPER PORT INTERFACE SECTION A (FIG. 11)
UPPER PORT INTERFACE SECTION B
UPPER PORT INTERFACE SECTION C
UPPER PORT INTERFACE SECTION D
RWA RXA RYA RZA GWA GXA GYA GZA
RWB RXB RYB RZB GWB GXB GYB GZB
RWC RXC RYC RZC GWC GXC GYC GZC
RWD RXD RYD RZD GWD GXD GYD GZD
CROSSBAR 50041
50061
50062
50063
50064
50061

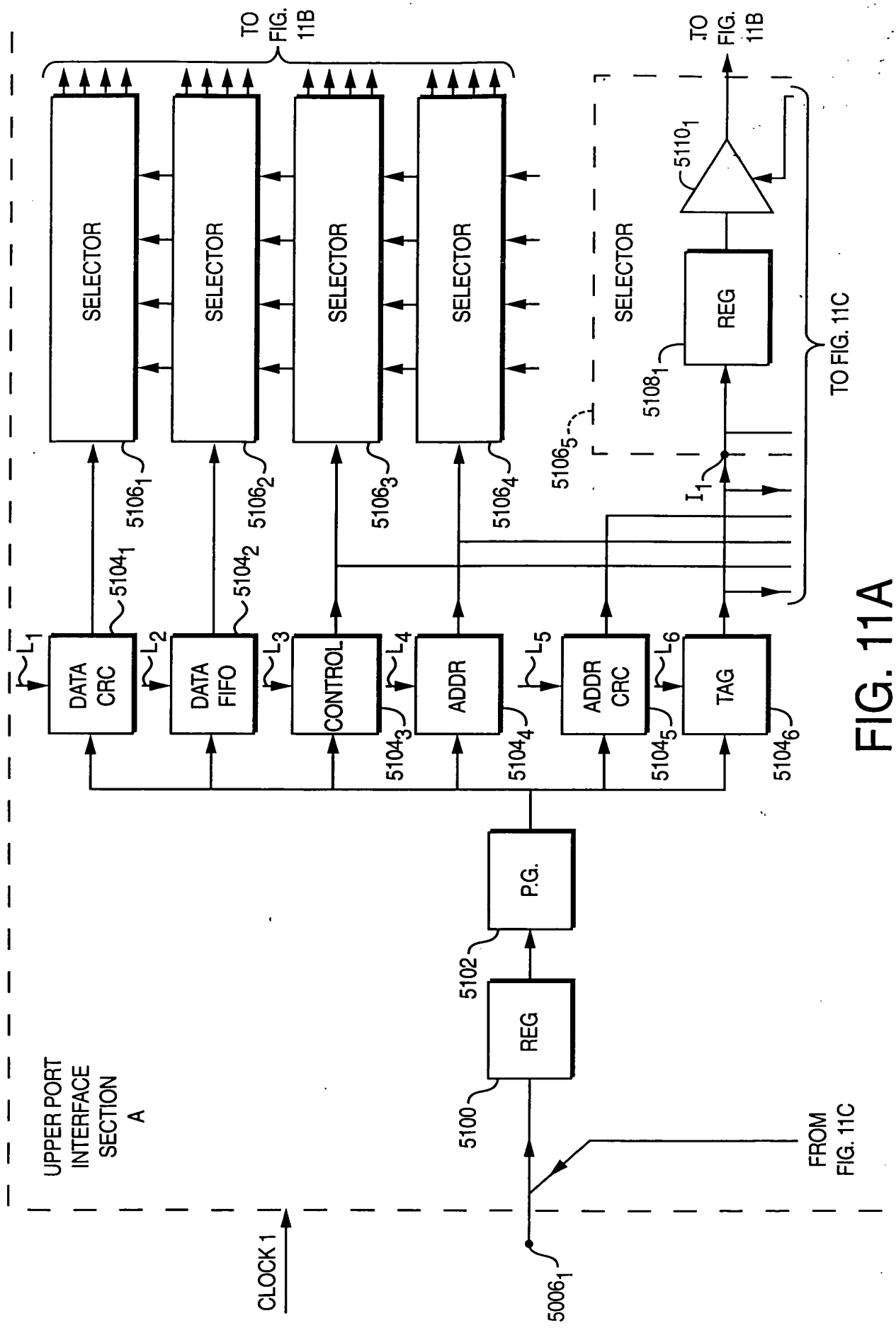

TO FIG. 11B
TO FIG. 11B
SELECTOR
SELECTOR
SELECTOR
SELECTOR
SELECTOR
REG
TO FIG. 11C
DATA CRC
DATA FIFO
CONTROL
ADDR
ADDR CRC
TAG
P.G.
REG
UPPER PORT INTERFACE SECTION A
FROM FIG. 11C
CLOCK 1

FIG. 11A

FIG. 11B

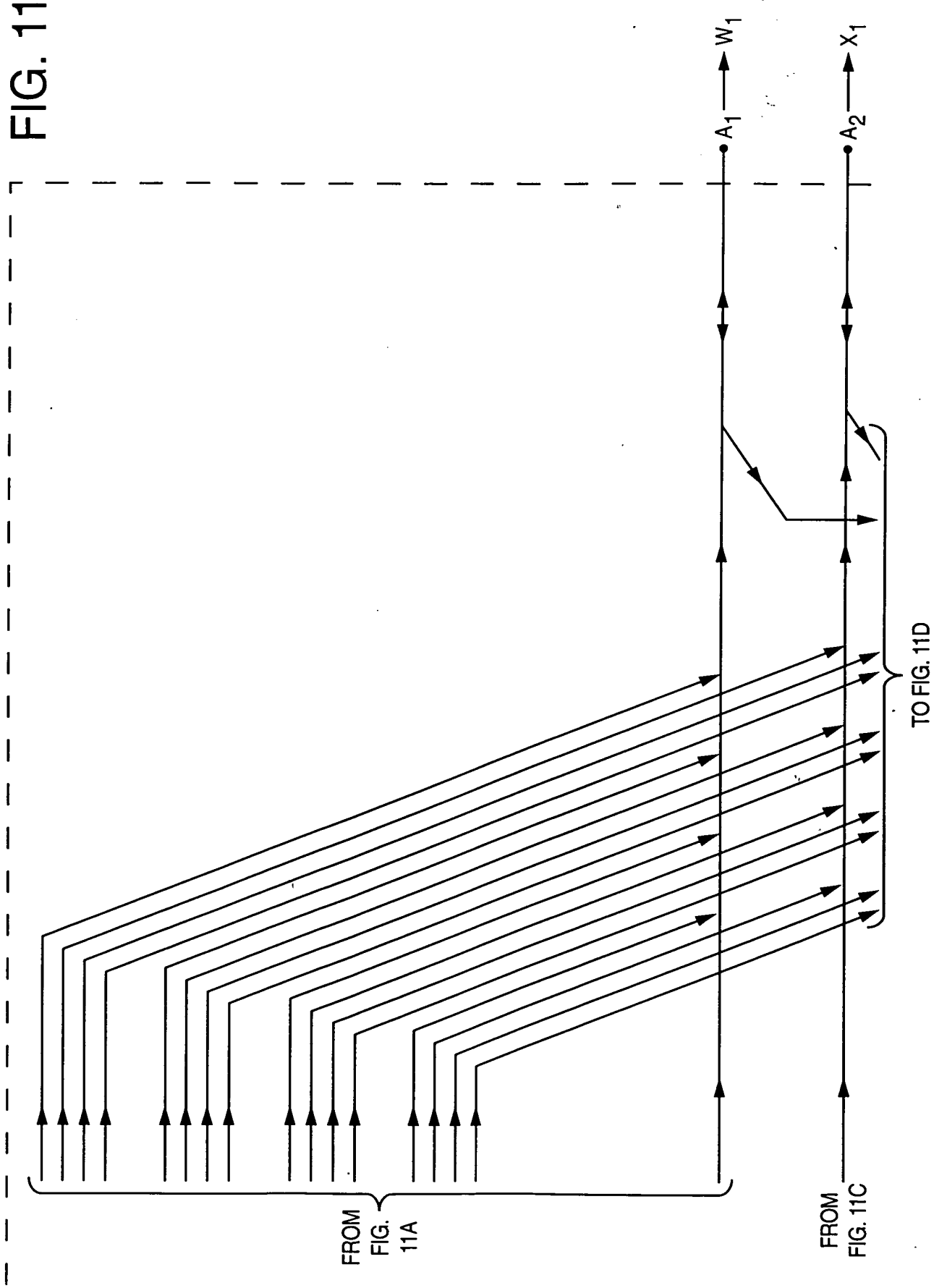
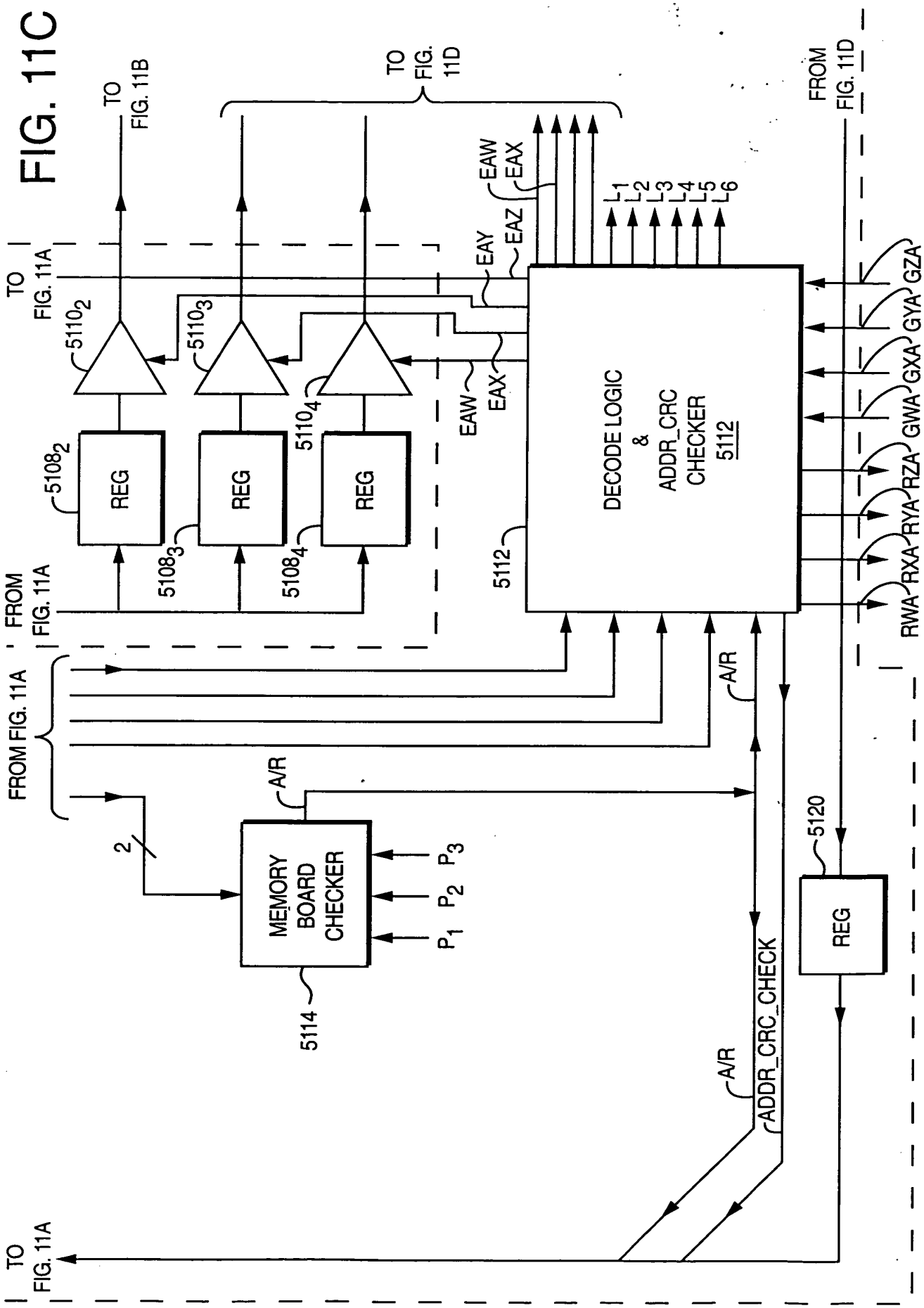


FIG. 11C


TO FIG. 11B
TO FIG. 11D
FROM FIG. 11D
TO FIG. 11A
FROM FIG. 11A
FROM FIG. 11A
TO FIG. 11A
5110$_2$
5110$_3$
5110$_4$
5108$_2$
5108$_3$
5108$_4$
REG
REG
REG
EAW
EAX
EAY
EAZ
L1
L2
L3
L4
L5
L6
DECODE LOGIC & ADDR_CRC CHECKER 5112
5112
GZA
GYA
GXA
GWA
RZA
RYA
RXA
RWA
A/R
A/R
A/R
2
MEMORY BOARD CHECKER
5114
P1 P2 P3
5120
REG
ADDR_CRC_CHECK

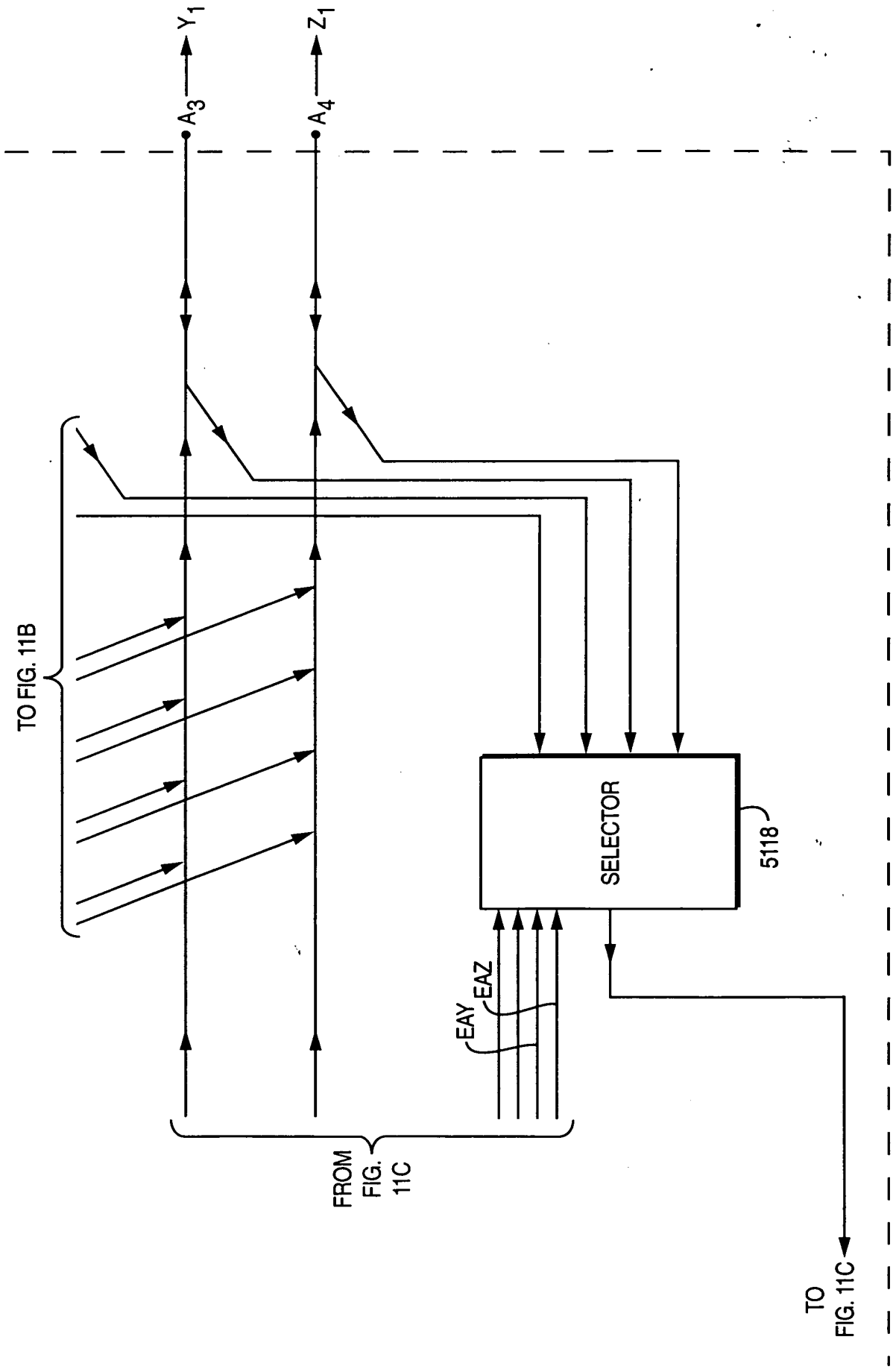

Y_1
Z_1
A_3
A_4
TO FIG. 11B
SELECTOR
5118
EAY
EAZ
FROM FIG. 11C
TO FIG. 11C

FIG. 11D

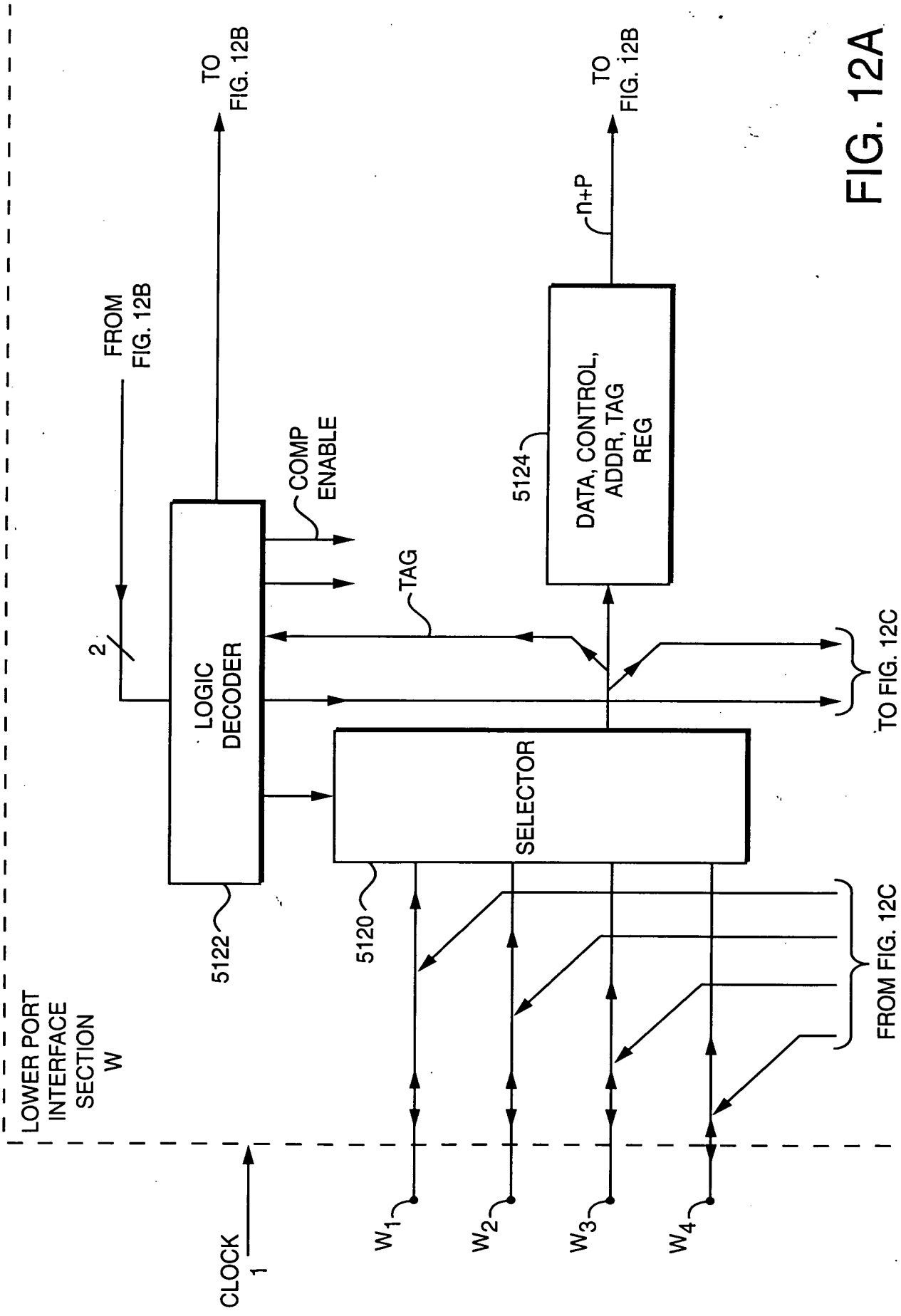

LOWER PORT INTERFACE SECTION W
CLOCK
1
FROM FIG. 12B
2
LOGIC DECODER
5122
TO FIG. 12B
COMP ENABLE
TAG
5120
SELECTOR
5124
DATA, CONTROL, ADDR, TAG REG
n+P
TO FIG. 12B
TO FIG. 12C
FROM FIG. 12C
W1
W2
W3
W4

FIG. 12A

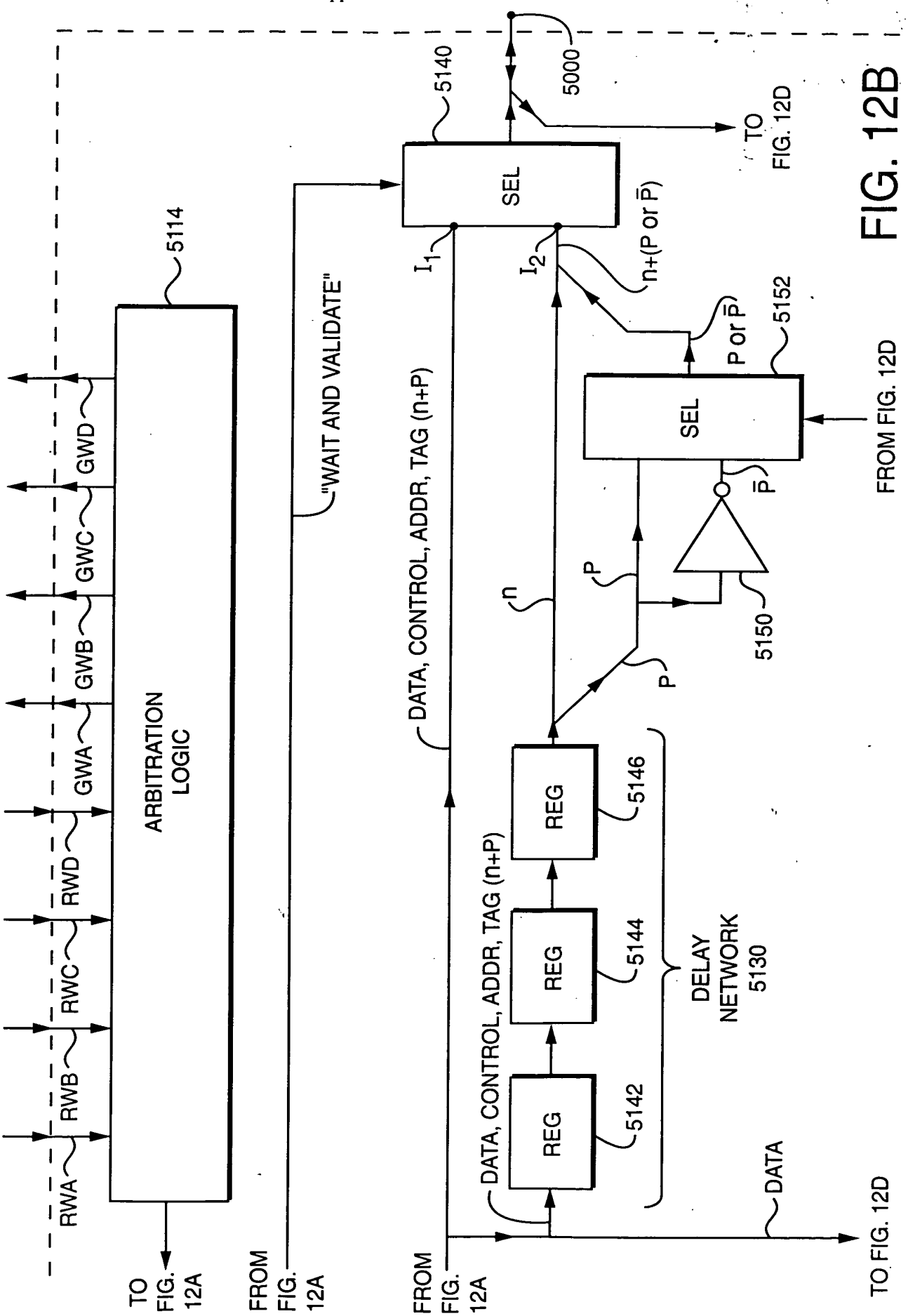

5114
ARBITRATION LOGIC
RWA
RWB
RWC
RWD
GWA
GWB
GWC
GWD
TO FIG. 12A
FROM FIG. 12A
"WAIT AND VALIDATE"
5140
SEL
5000
TO FIG. 12D
I_1
I_2
n+(P or $\bar{P}$)
DATA, CONTROL, ADDR, TAG (n+P)
5152
SEL
P or $\bar{P}$
FROM FIG. 12D
$\bar{P}$
n
P
P
5150
REG
5146
REG
5144
REG
5142
DELAY NETWORK 5130
DATA, CONTROL, ADDR, TAG (n+P)
FROM FIG. 12A
DATA
TO FIG. 12D

FIG. 12B

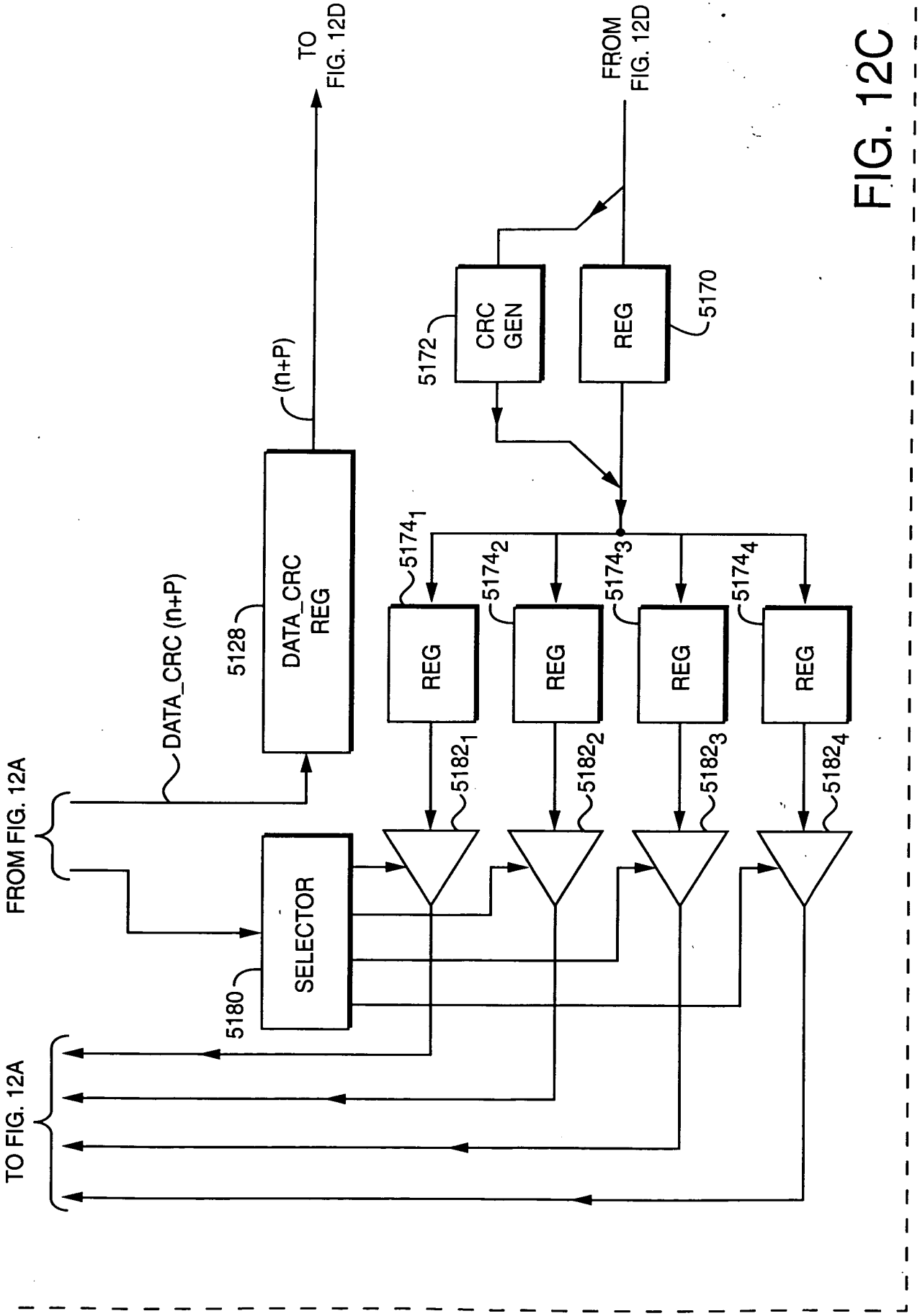

TO FIG. 12D
FROM FIG. 12D
(n+P)
5172
CRC GEN
REG
5170
5174$_1$
5174$_2$
5174$_3$
5174$_4$
DATA_CRC (n+P)
5128
DATA_CRC REG
REG
REG
REG
REG
5182$_1$
5182$_2$
5182$_3$
5182$_4$
FROM FIG. 12A
SELECTOR
5180
TO FIG. 12A

FIG. 12C

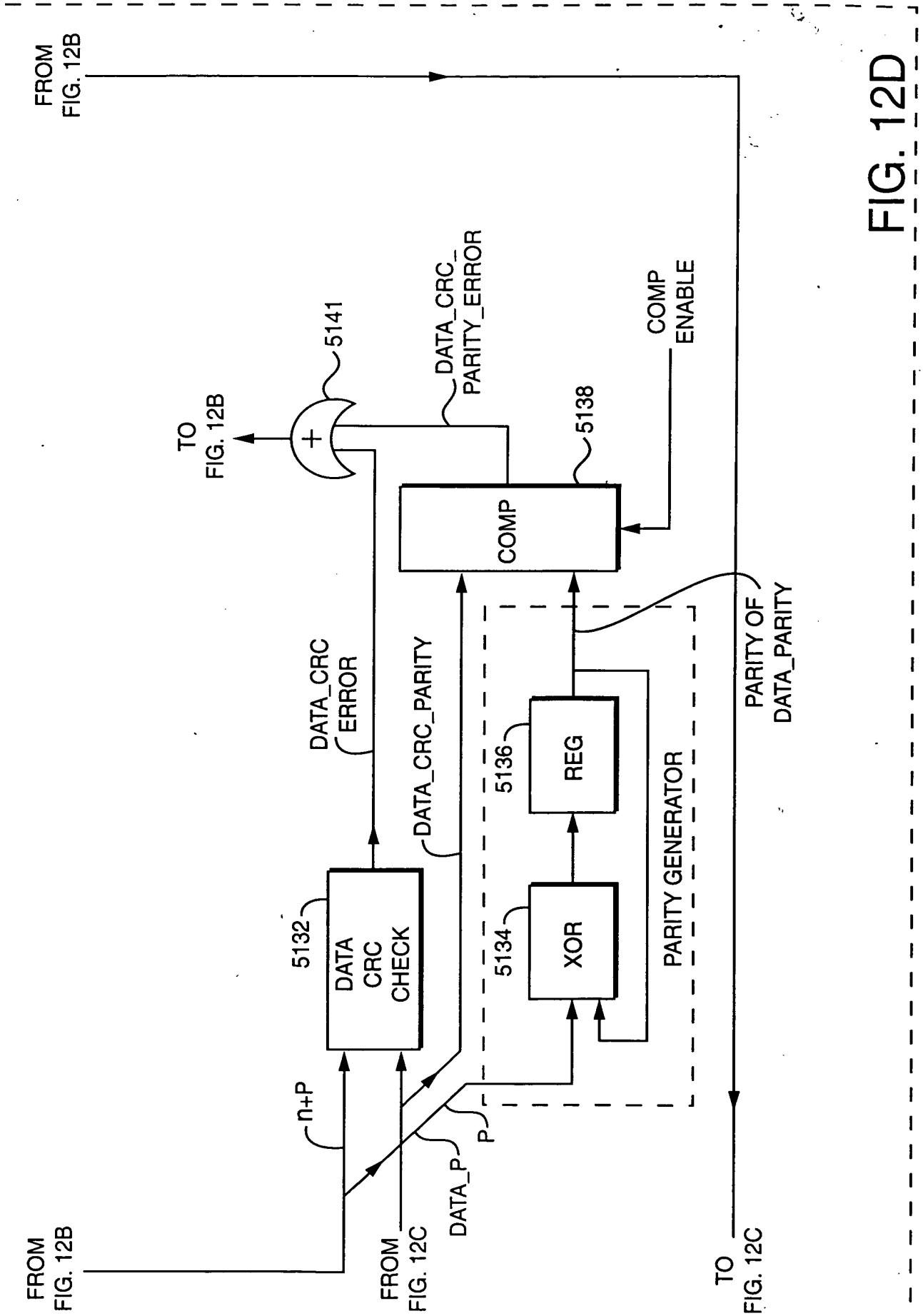

FROM FIG. 12B
TO FIG. 12B
5141
DATA_CRC_ PARITY_ERROR
COMP ENABLE
5138
COMP
DATA_CRC ERROR
DATA_CRC_PARITY
5136
REG
PARITY OF DATA_PARITY
PARITY GENERATOR
5132
DATA CRC CHECK
5134
XOR
n+P
P
DATA_P
FROM FIG. 12B
FROM FIG. 12C
TO FIG. 12C

FIG. 12D

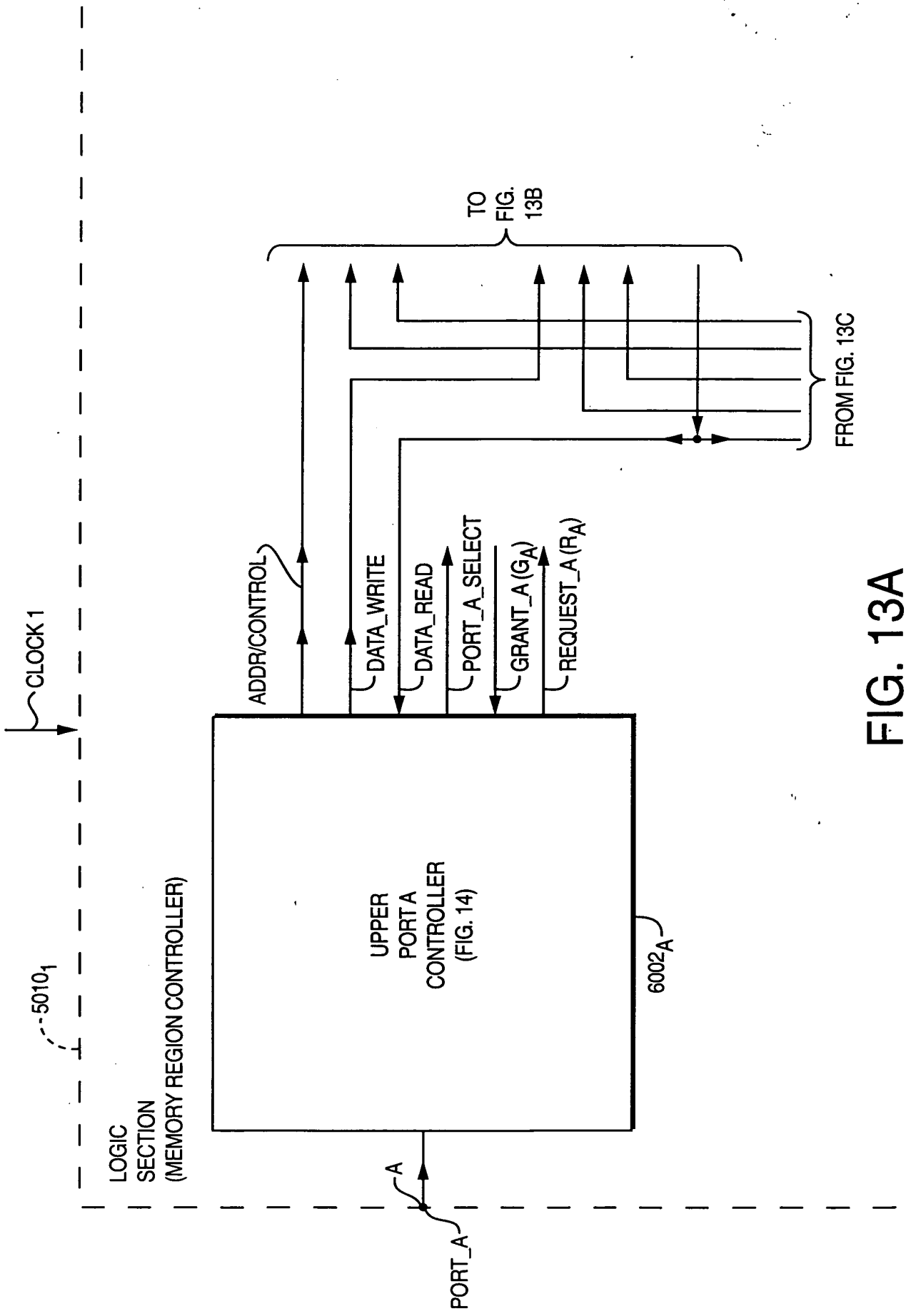

LOGIC SECTION (MEMORY REGION CONTROLLER)
5010$_1$
CLOCK 1
PORT_A
A
UPPER PORT A CONTROLLER (FIG. 14)
6002$_A$
ADDR/CONTROL
DATA_WRITE
DATA_READ
PORT_A_SELECT
GRANT_A (G_A)
REQUEST_A (R_A)
TO FIG. 13B
FROM FIG. 13C

FIG. 13A

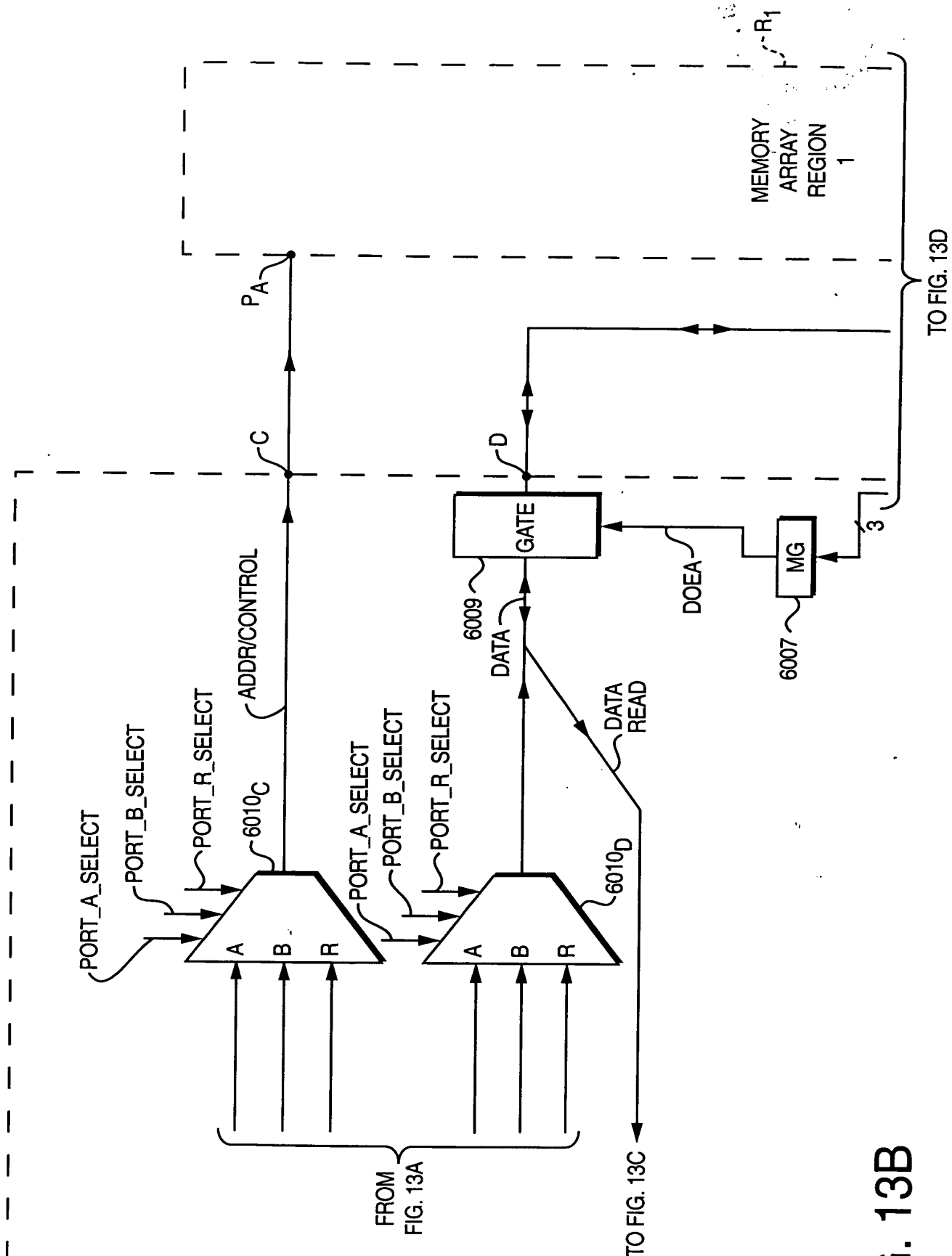

MEMORY ARRAY REGION 1
R_1
TO FIG. 13D
P_A
C
D
GATE
6009
DATA
DOEA
MG
6007
3
ADDR/CONTROL
PORT_A_SELECT
PORT_B_SELECT
PORT_R_SELECT
6010_C
PORT_A_SELECT
PORT_B_SELECT
PORT_R_SELECT
6010_D
DATA READ
A
B
R
A
B
R
FROM FIG. 13A
TO FIG. 13C

FIG. 13B

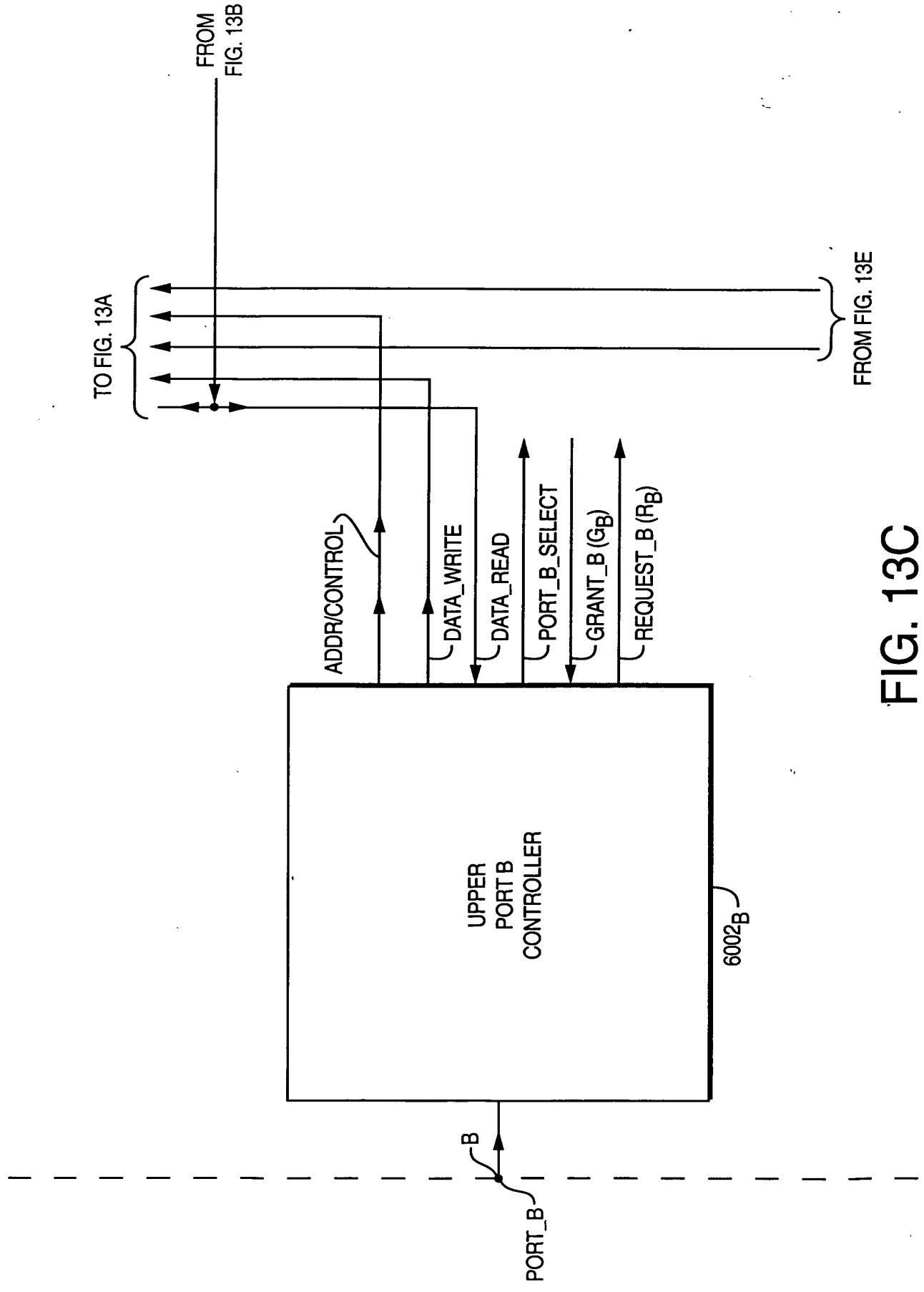

FROM FIG. 13B
TO FIG. 13A
FROM FIG. 13E
ADDR/CONTROL
DATA_WRITE
DATA_READ
PORT_B_SELECT
GRANT_B (G_B)
REQUEST_B (R_B)
UPPER PORT B CONTROLLER
6002_B
B
PORT_B

FIG. 13C

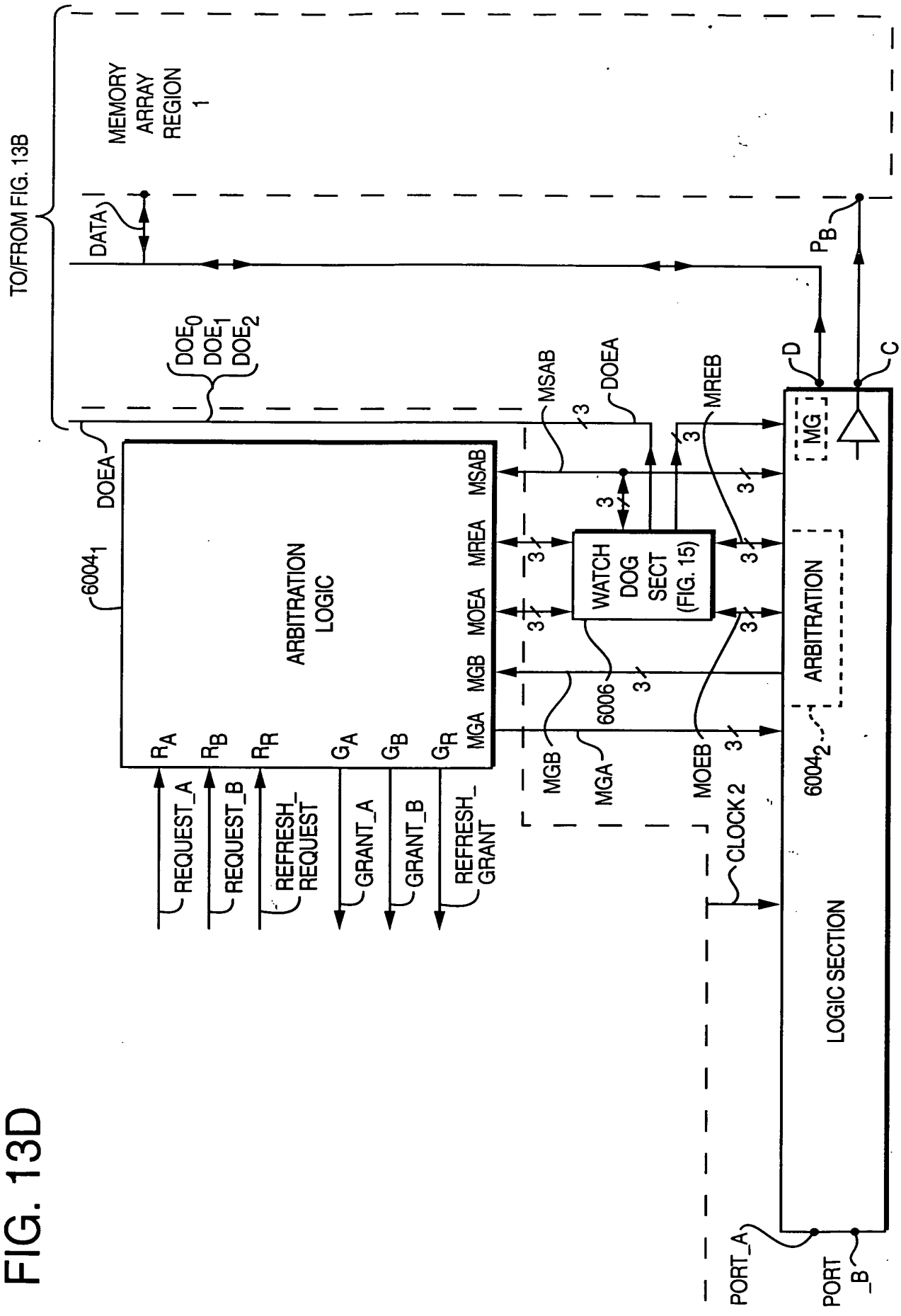

TO/FROM FIG. 13B
MEMORY ARRAY REGION 1
DATA
P_B
DOE_0 DOE_1 DOE_2
DOEA
MSAB
DOEA
MREB
D
C
MG
6004_1
ARBITRATION LOGIC
MSAB
MREA
MOEA
MGB
MGA
WATCH DOG SECT (FIG. 15)
6006
ARBITRATION
6004_2
R_A R_B R_R G_A G_B G_R
REQUEST_A
REQUEST_B
REFRESH_ REQUEST
GRANT_A
GRANT_B
REFRESH_ GRANT
MGB
MGA
MOEB
CLOCK 2
LOGIC SECTION
PORT_A
PORT_B

FIG. 13D

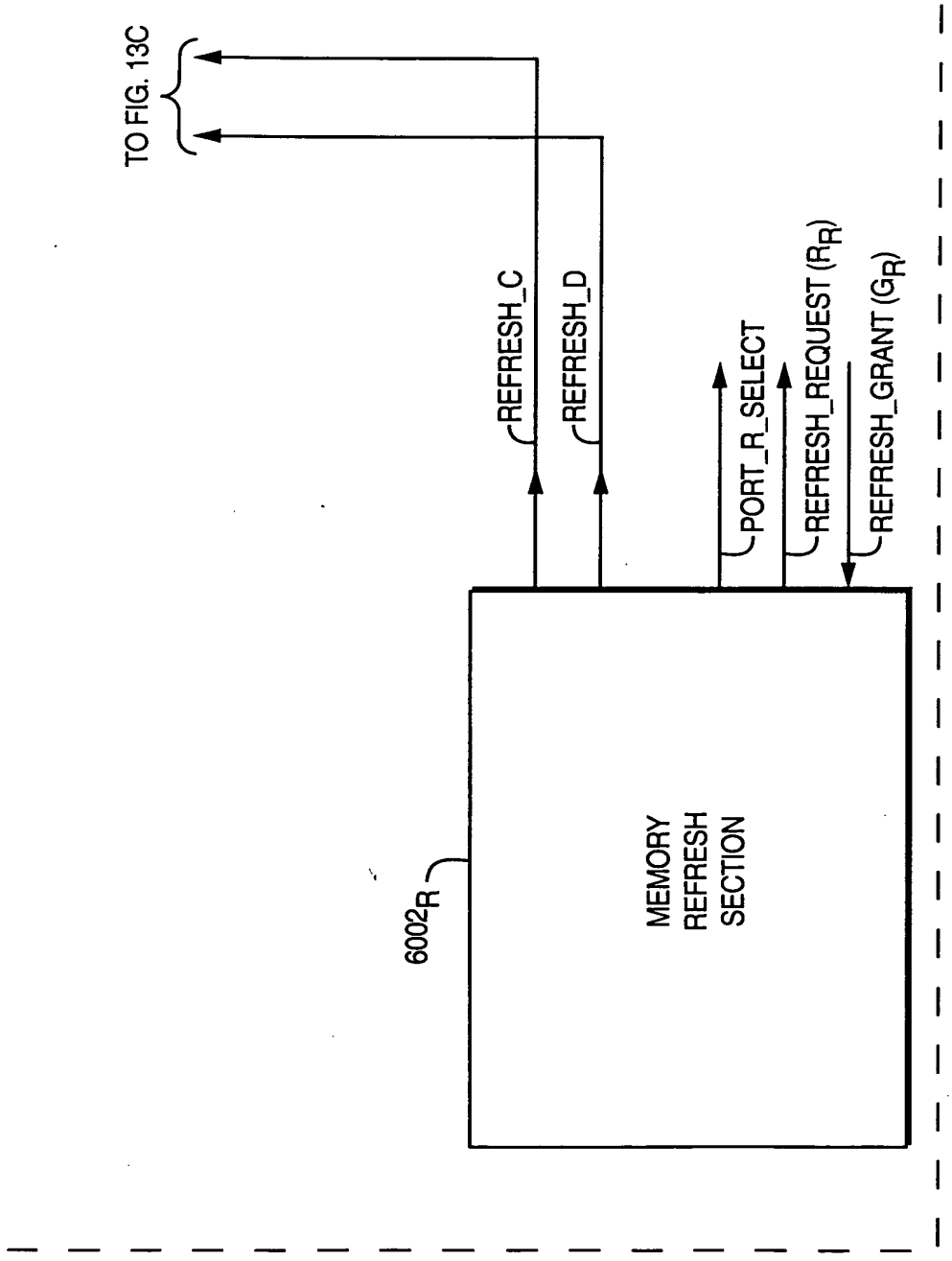

TO FIG. 13C
REFRESH_C
REFRESH_D
PORT_R_SELECT
REFRESH_REQUEST (R_R)
REFRESH_GRANT (G_R)
MEMORY REFRESH SECTION
6002_R

FIG. 13E

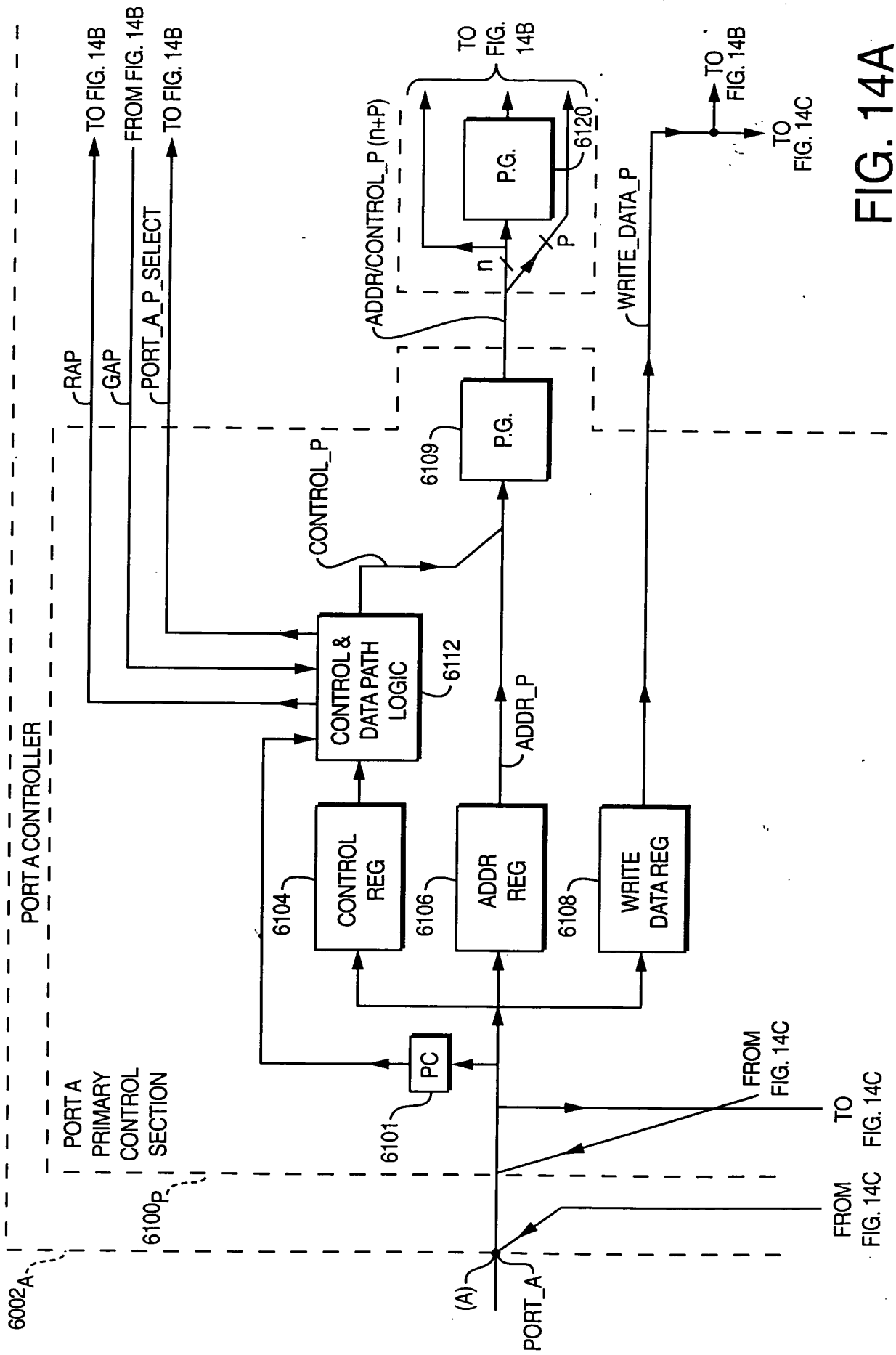

6002A
PORT A CONTROLLER
PORT A PRIMARY CONTROL SECTION
6100P
PC
6101
CONTROL REG
6104
ADDR REG
6106
WRITE DATA REG
6108
CONTROL & DATA PATH LOGIC
6112
P.G.
6109
P.G.
6120
RAP
GAP
PORT_A_P_SELECT
CONTROL_P
ADDR_P
ADDR/CONTROL_P (n+P)
WRITE_DATA_P
n
P
TO FIG. 14B
FROM FIG. 14B
TO FIG. 14B
TO FIG. 14B
TO FIG. 14B
TO FIG. 14C
FROM FIG. 14C
TO FIG. 14C
FROM FIG. 14C
(A)
PORT_A

FIG. 14A

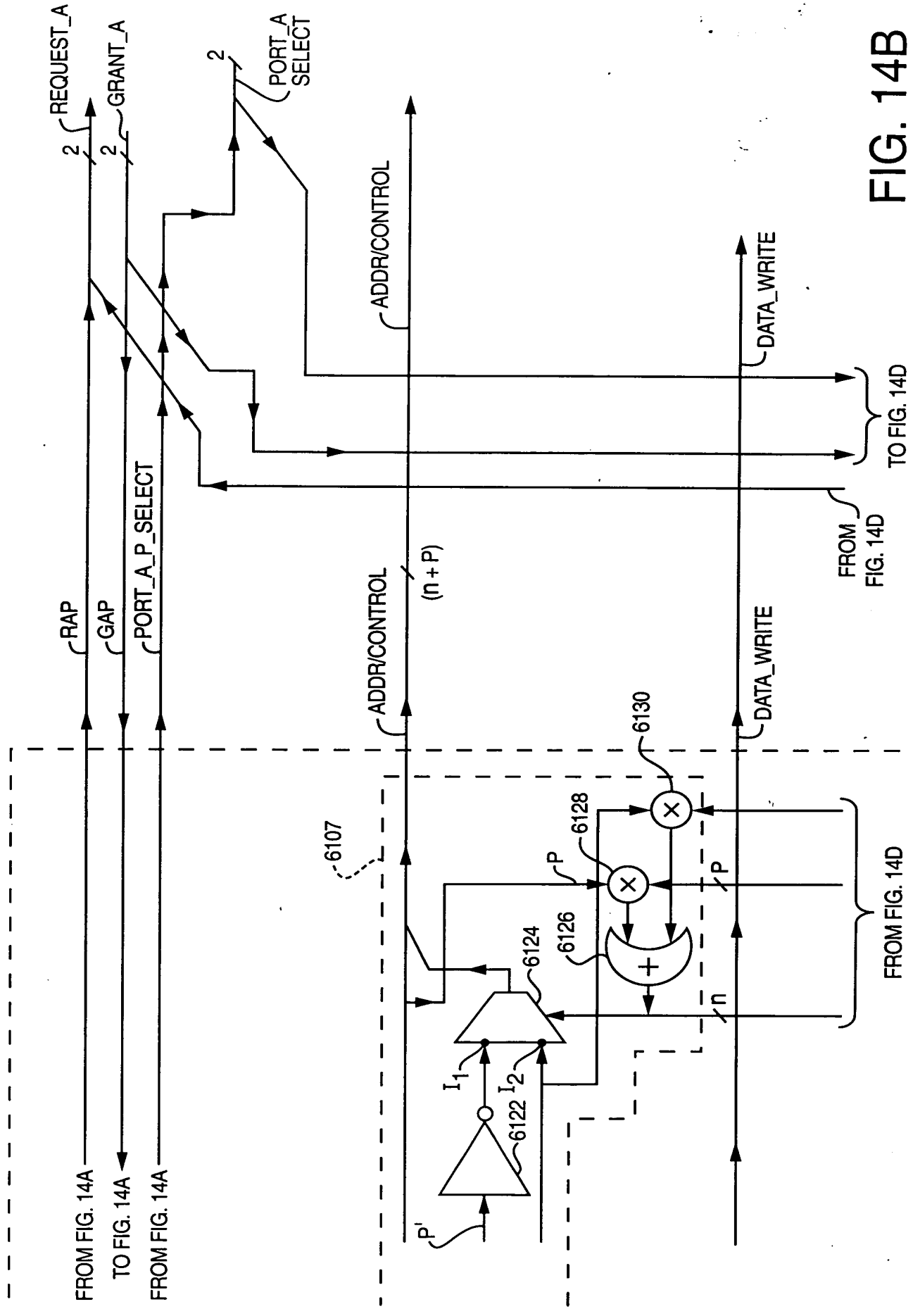

REQUEST_A
GRANT_A
2
2
PORT_A SELECT
ADDR/CONTROL
DATA_WRITE
TO FIG. 14D
FROM FIG. 14D
RAP
GAP
PORT_A_P_SELECT
ADDR/CONTROL
(n + P)
DATA_WRITE
6130
6128
6107
P
P
6124
6126
n
I_1
I_2
6122
P'
FROM FIG. 14A
TO FIG. 14A
FROM FIG. 14A
FROM FIG. 14D

FIG. 14B

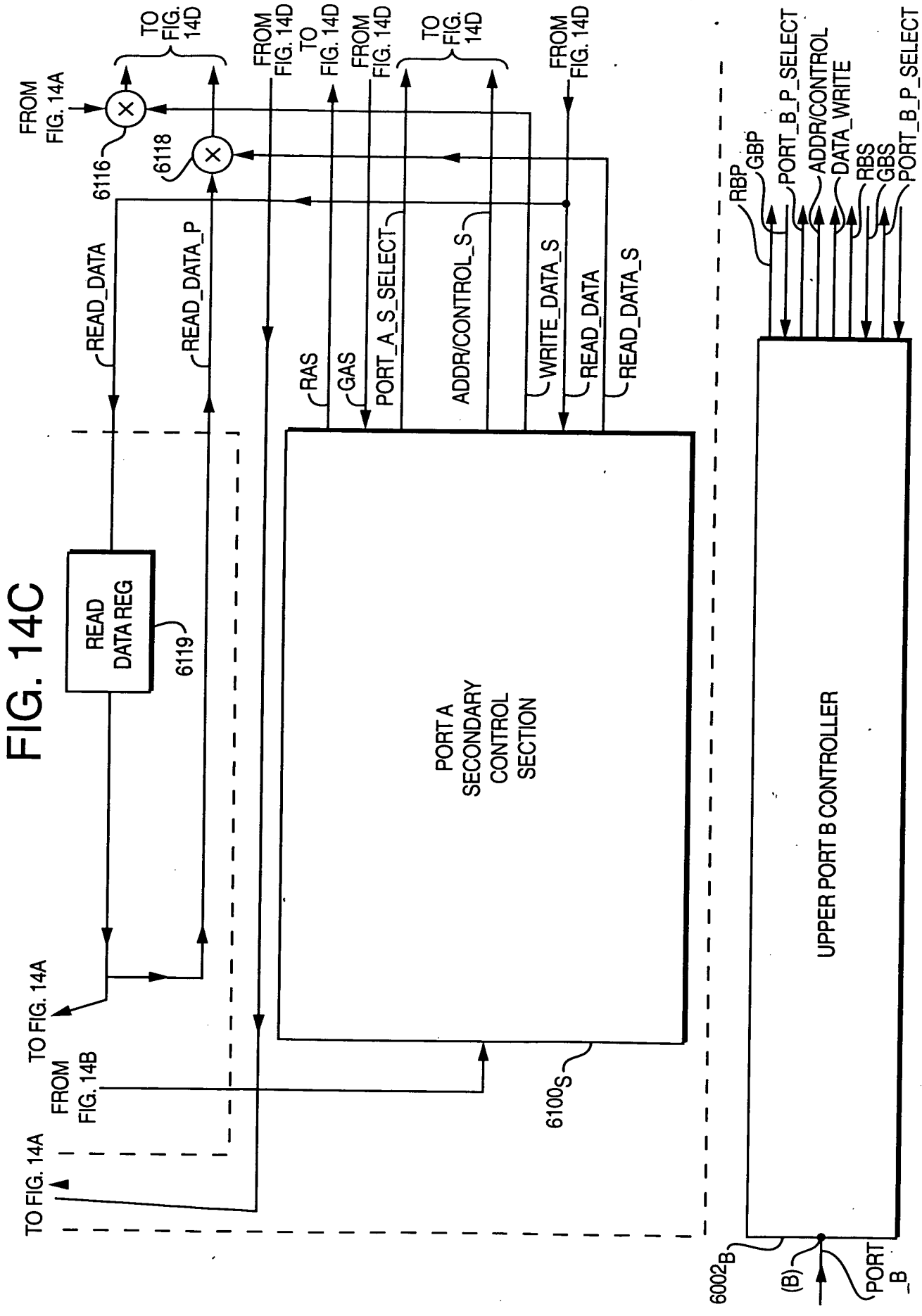

FROM FIG. 14A
TO FIG. 14D
FROM FIG. 14D
TO FIG. 14D
FROM FIG. 14D
TO FIG. 14D
FROM FIG. 14D
6116
6118
READ_DATA
READ_DATA_P
RAS
GAS
PORT_A_S_SELECT
ADDR/CONTROL_S
WRITE_DATA_S
READ_DATA
READ_DATA_S
RBP
GBP
PORT_B_P_SELECT
ADDR/CONTROL
DATA_WRITE
RBS
GBS
PORT_B_P_SELECT
READ DATA REG
6119
PORT A SECONDARY CONTROL SECTION
UPPER PORT B CONTROLLER
TO FIG. 14A
FROM FIG. 14B
TO FIG. 14A
6100S
6002B
(B)
PORT B

FIG. 14C

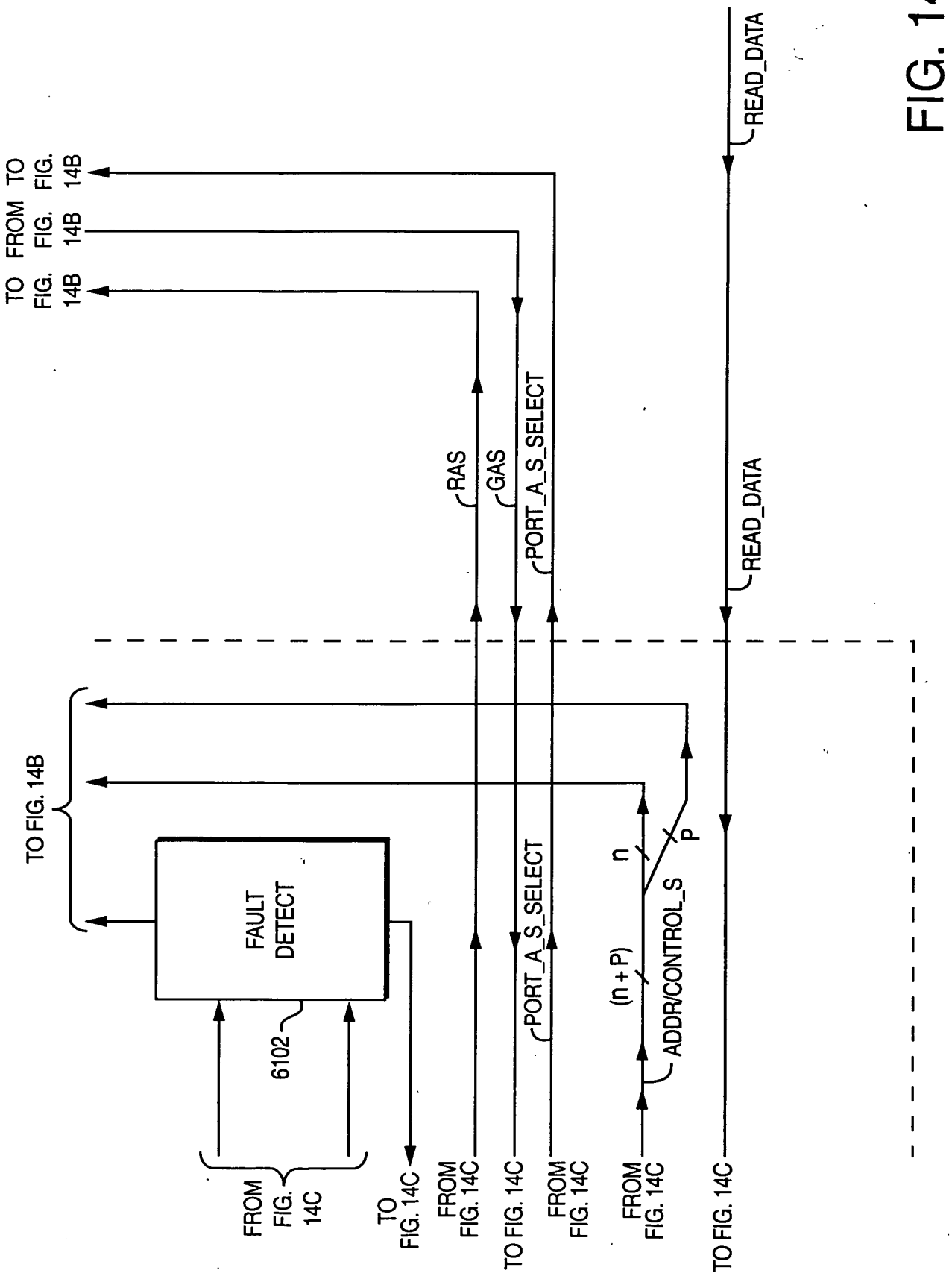

TO FIG. 14B
TO FROM TO FIG. 14B
TO FIG. 14B
READ_DATA
RAS
GAS
PORT_A_S_SELECT
READ_DATA
FAULT DETECT
6102
FROM FIG. 14C
TO FIG. 14C
FROM FIG. 14C
TO FIG. 14C
FROM FIG. 14C
(n+P)
n
P
ADDR/CONTROL_S
FROM FIG. 14C
TO FIG. 14C

FIG. 14D

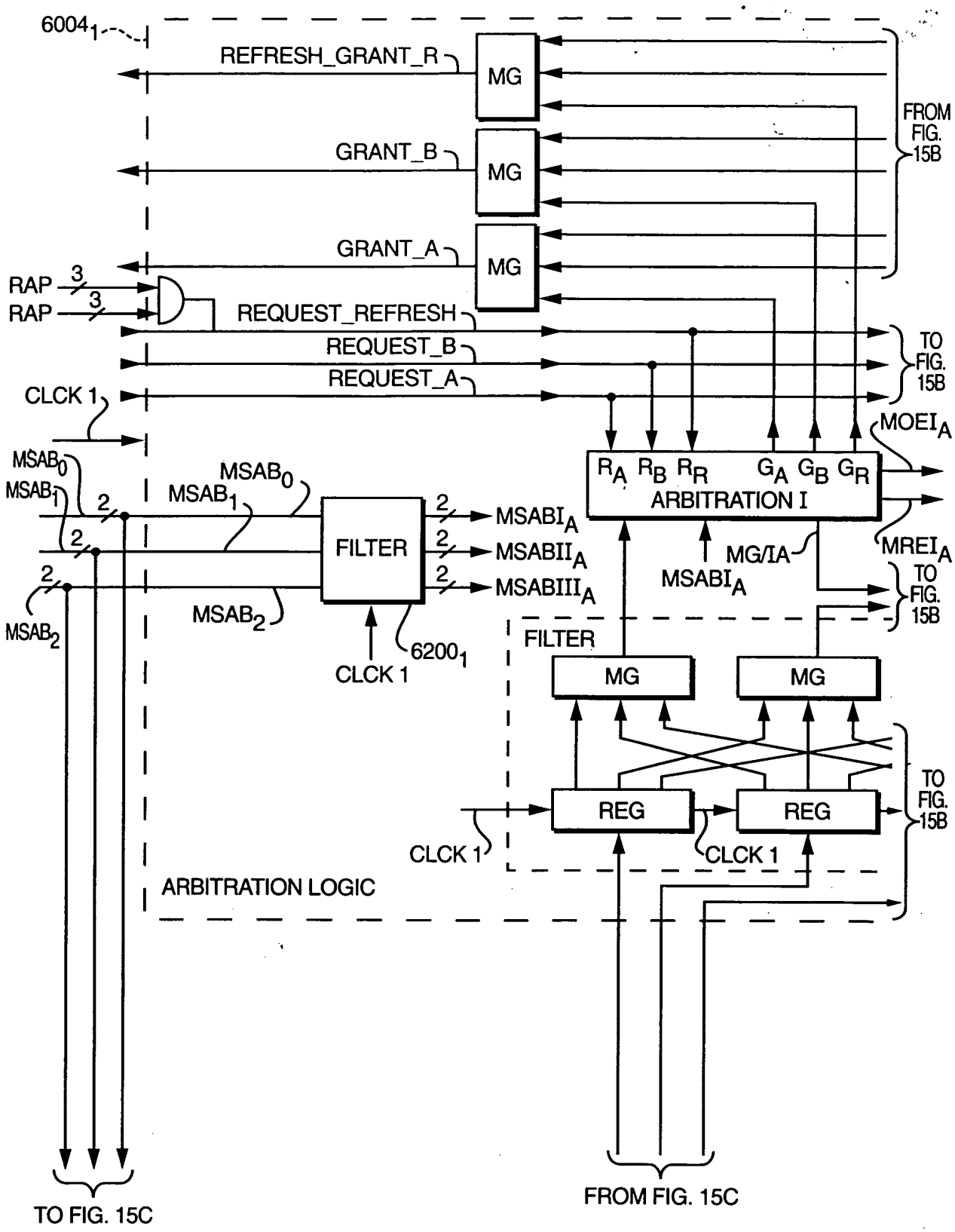

6004 1
REFRESH_GRANT_R
GRANT_B
GRANT_A
MG
MG
MG
FROM FIG. 15B
RAP 3
RAP 3
REQUEST_REFRESH
REQUEST_B
REQUEST_A
TO FIG. 15B
CLCK 1
MOEI A
MSAB 0
MSAB 1
MSAB 2
2
2
2
FILTER
MSABI A
MSABII A
MSABIII A
MSAB 0
MSAB 1
MSAB 2
6200 1
CLCK 1
R A R B R R G A G B G R
ARBITRATION I
MG/IA
MSABI A
MREI A
TO FIG. 15B
FILTER
MG
MG
REG
REG
CLCK 1
CLCK 1
TO FIG. 15B
ARBITRATION LOGIC
TO FIG. 15C
FROM FIG. 15C

FIG. 15A

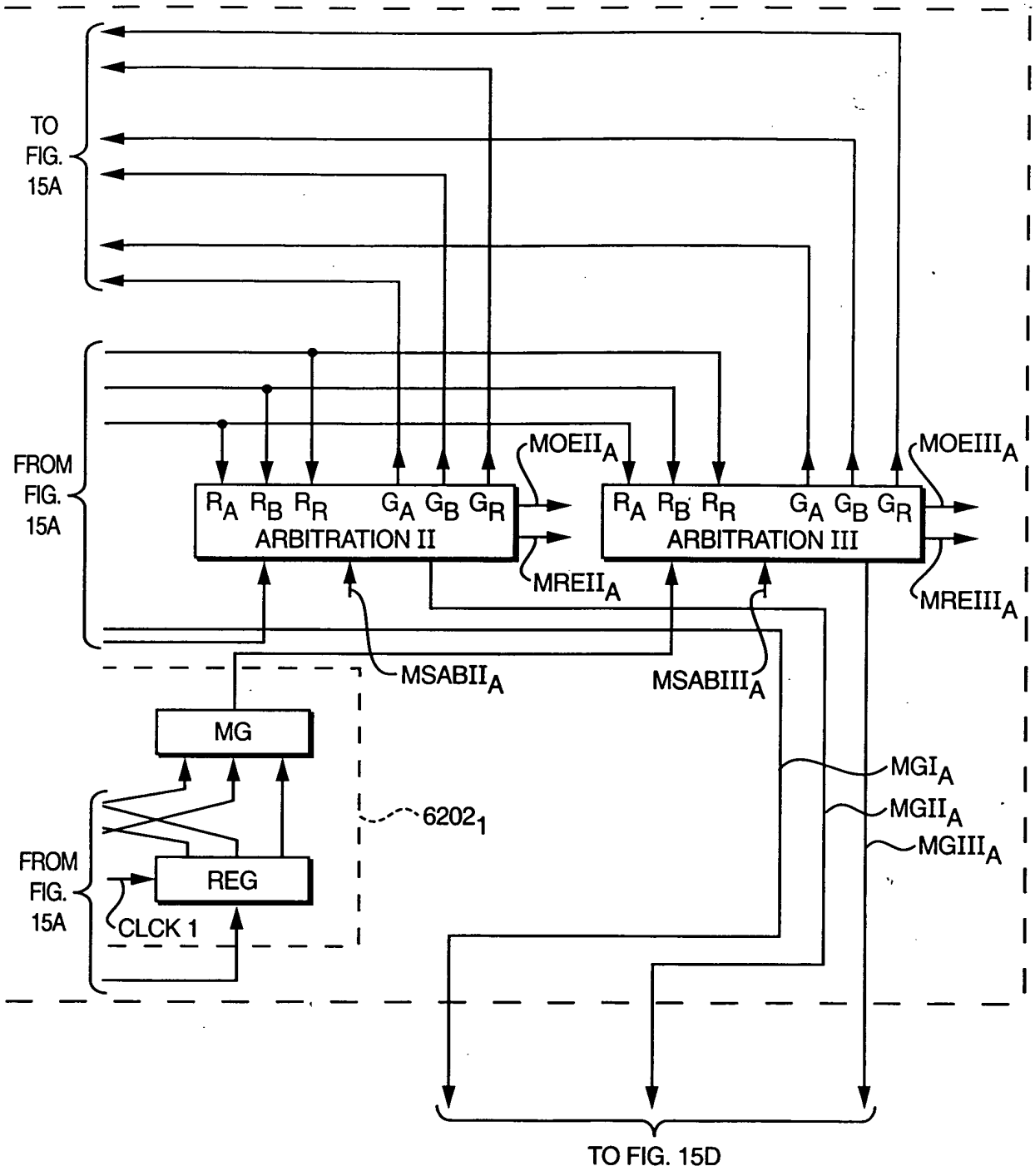

TO FIG. 15A
FROM FIG. 15A
R_A R_B R_R G_A G_B G_R
ARBITRATION II
ARBITRATION III
$MOEII_A$
$MOEIII_A$
$MREII_A$
$MREIII_A$
$MSABII_A$
$MSABIII_A$
MG
REG
CLCK 1
6202_1
FROM FIG. 15A
MGI_A
$MGII_A$
$MGIII_A$
TO FIG. 15D

FIG. 15B

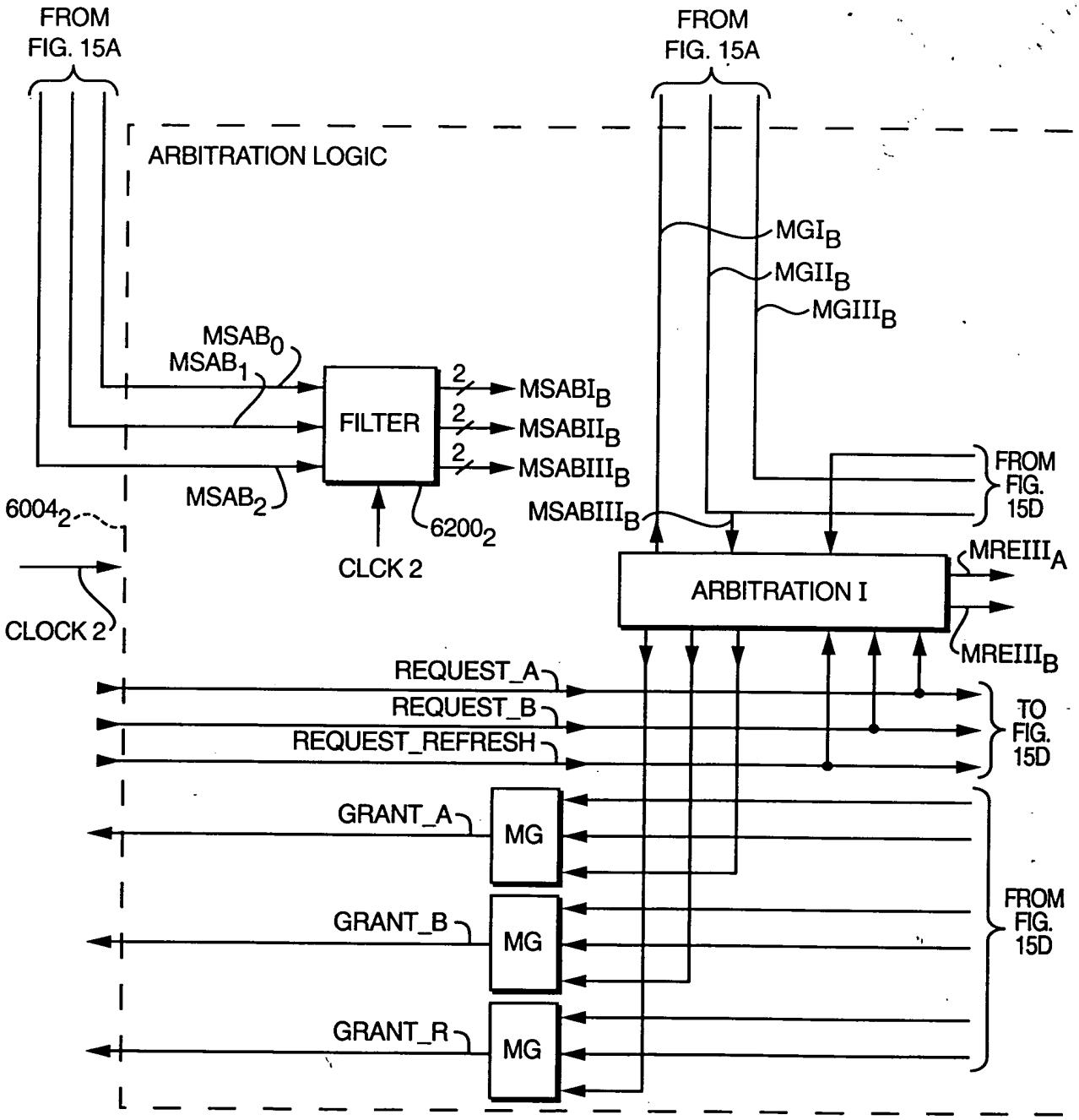

FROM FIG. 15A
FROM FIG. 15A
ARBITRATION LOGIC
MGI$_B$
MGII$_B$
MGIII$_B$
MSAB$_0$
MSAB$_1$
FILTER
2
MSABI$_B$
2
MSABII$_B$
2
MSABIII$_B$
MSAB$_2$
6004$_2$
6200$_2$
CLCK 2
MSABIII$_B$
FROM FIG. 15D
MREIII$_A$
ARBITRATION I
MREIII$_B$
CLOCK 2
REQUEST_A
REQUEST_B
REQUEST_REFRESH
TO FIG. 15D
GRANT_A
MG
GRANT_B
MG
GRANT_R
MG
FROM FIG. 15D

FIG. 15C

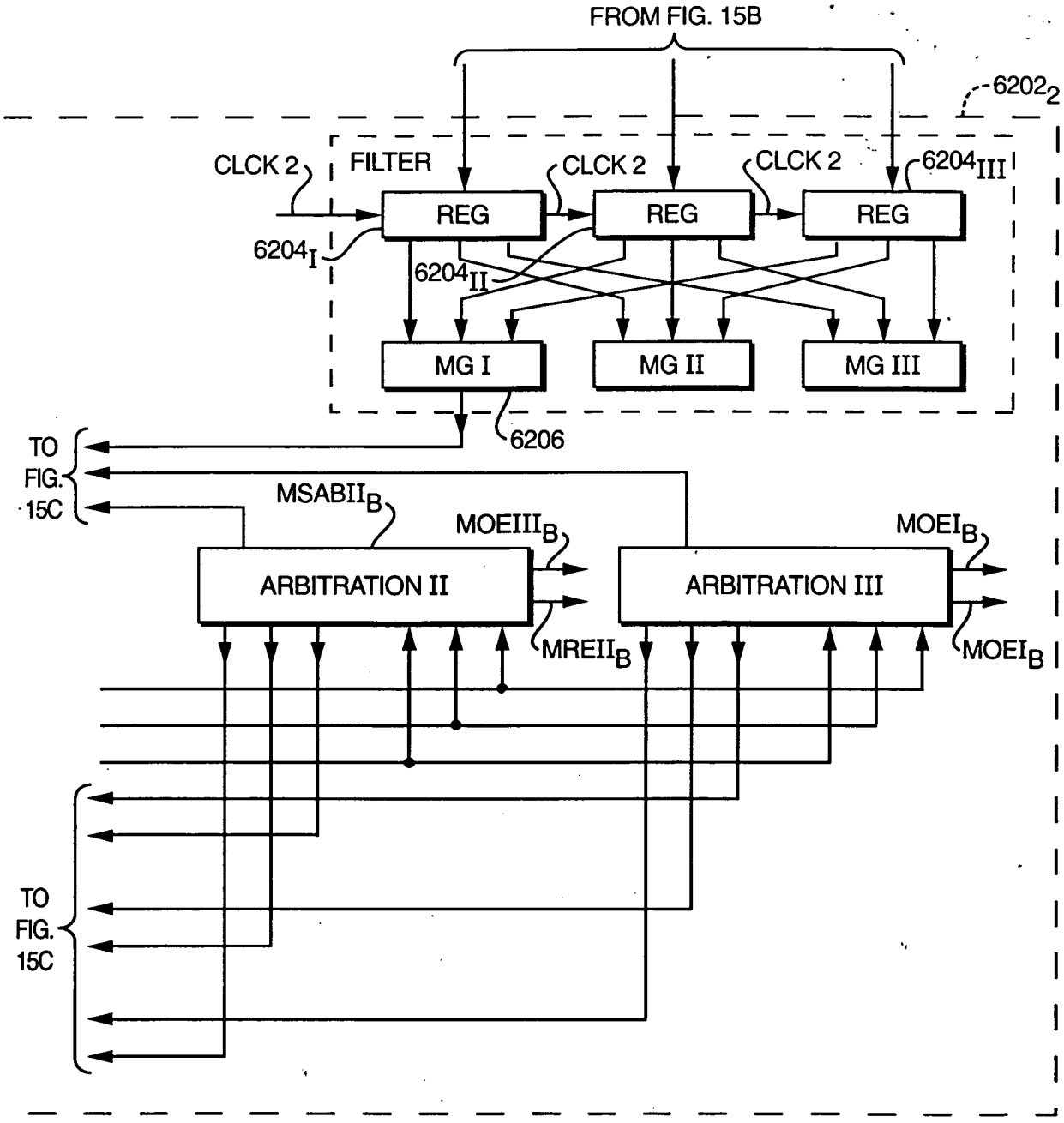

FROM FIG. 15B
6202$_2$
FILTER
CLCK 2
CLCK 2
CLCK 2
6204$_{III}$
REG
REG
REG
6204$_I$
6204$_{II}$
MG I
MG II
MG III
6206
TO FIG. 15C
MSABII$_B$
MOEIII$_B$
MOEI$_B$
ARBITRATION II
ARBITRATION III
MREII$_B$
MOEI$_B$
TO FIG. 15C

FIG. 15D

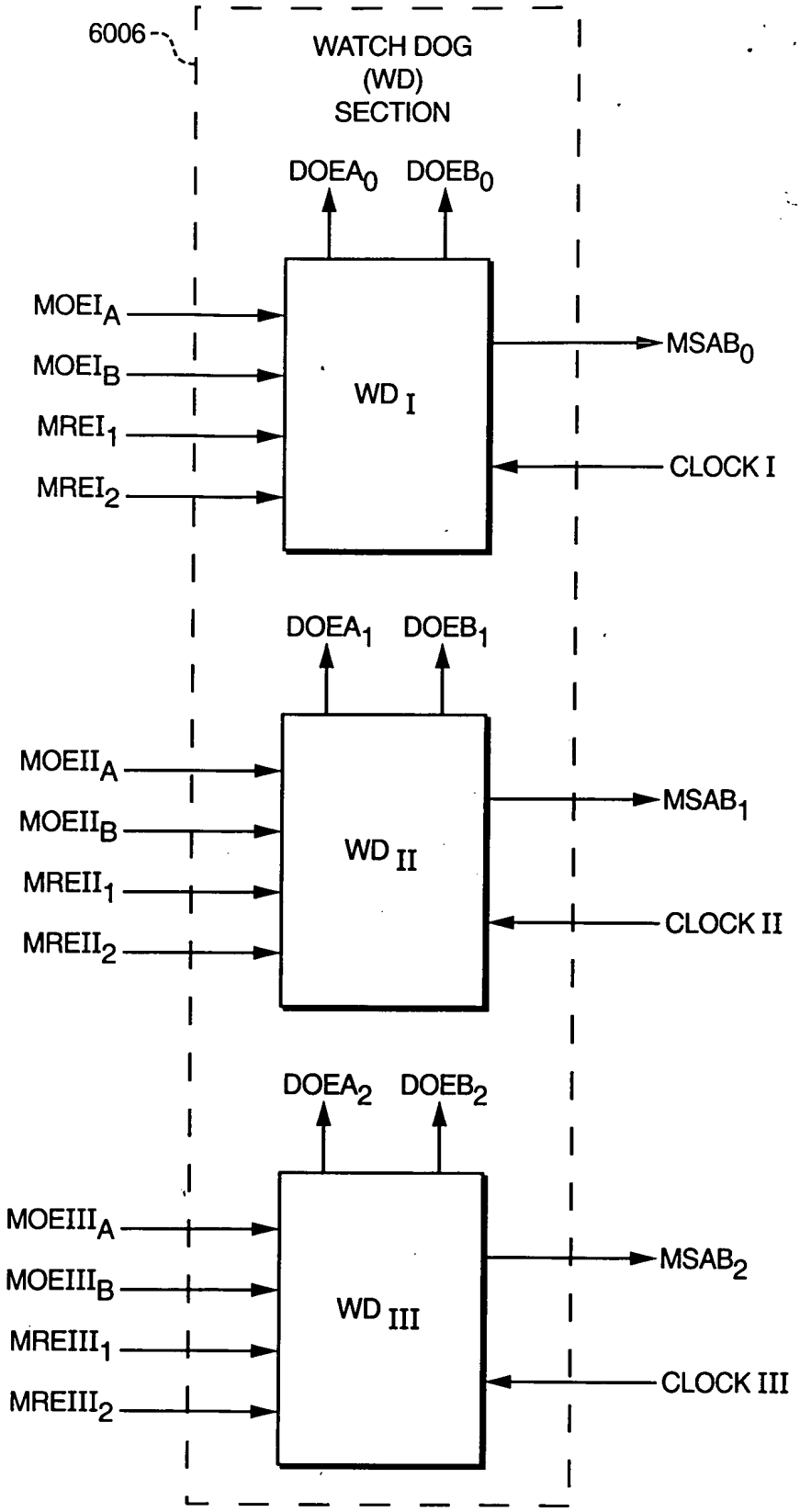

6006
WATCH DOG (WD) SECTION
DOEA0
DOEB0
MOEIA
MOEIB
MREI1
MREI2
WD I
MSAB0
CLOCK I
DOEA1
DOEB1
MOEIIA
MOEIIB
MREII1
MREII2
WD II
MSAB1
CLOCK II
DOEA2
DOEB2
MOEIIIA
MOEIIIB
MREIII1
MREIII2
WD III
MSAB2
CLOCK III

FIG. 15E

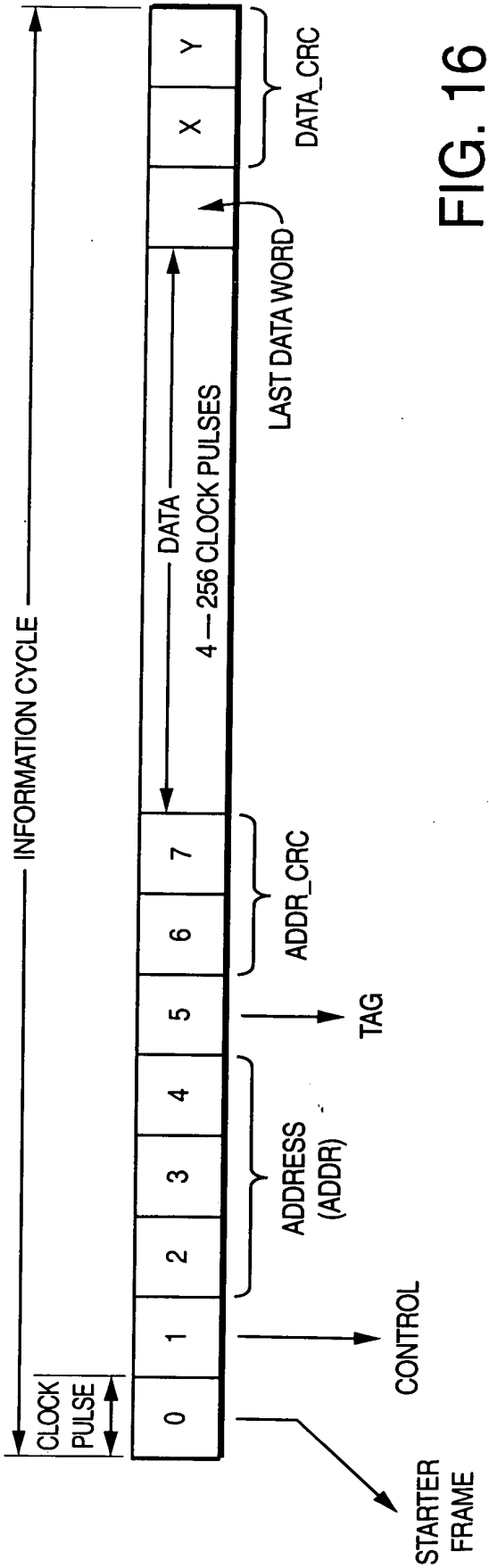


FIG. 16

MG INPUTS	MG OUTPUT	MG OUTPUT	MG OUTPUT
000	0	0	0
001	0	0	0
010	0	0	0
011	1	1	1
100	0	0	0
101	1	1	1
110	1	1	1
111	1	1	1

FIG. 17

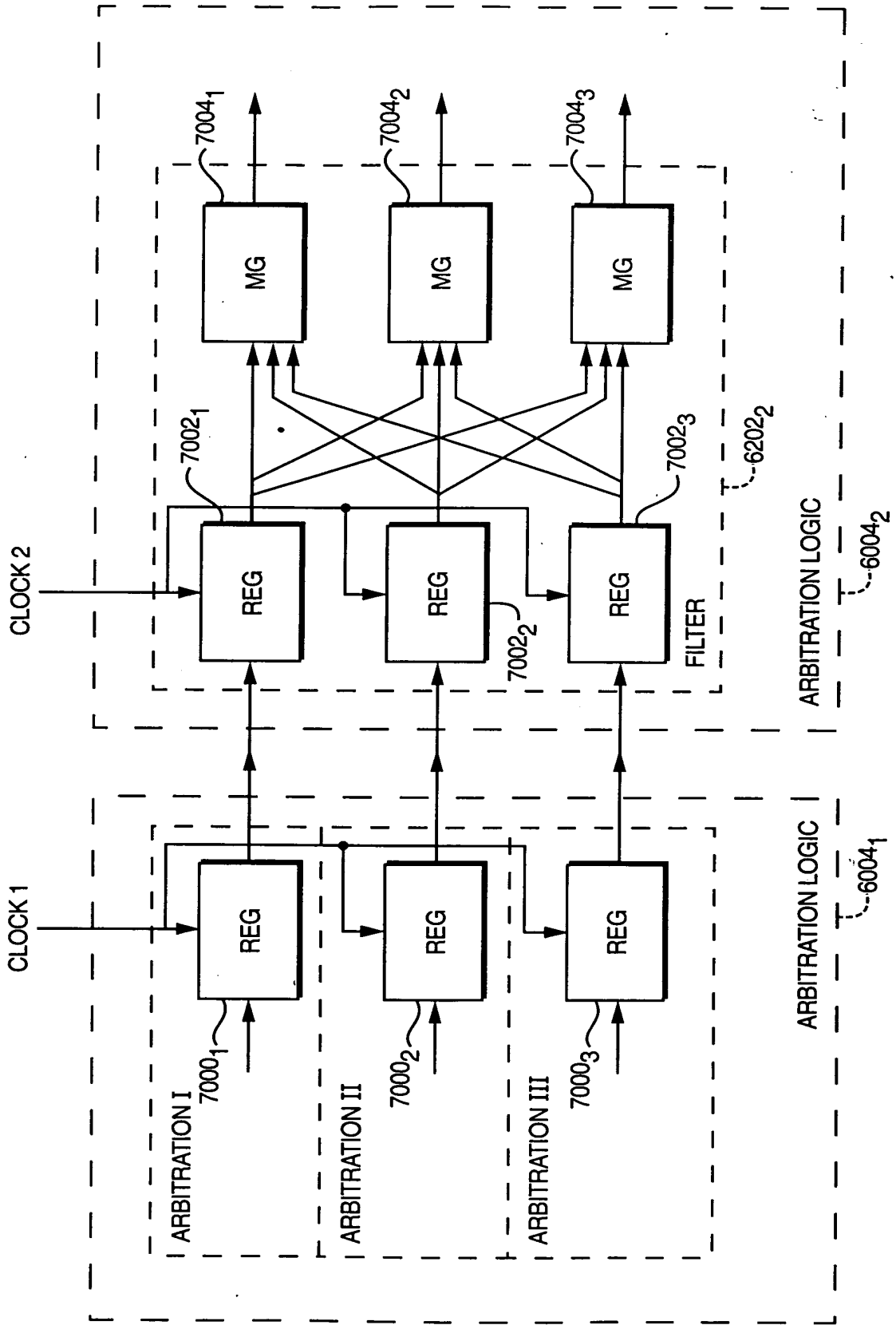

CLOCK 2
CLOCK 1
REG
REG
REG
REG
REG
REG
MG
MG
MG
7004_1
7004_2
7004_3
7002_1
7002_2
7002_3
6202_2
FILTER
ARBITRATION LOGIC
6004_2
ARBITRATION LOGIC
6004_1
ARBITRATION I
ARBITRATION II
ARBITRATION III
7000_1
7000_2
7000_3

FIG. 18

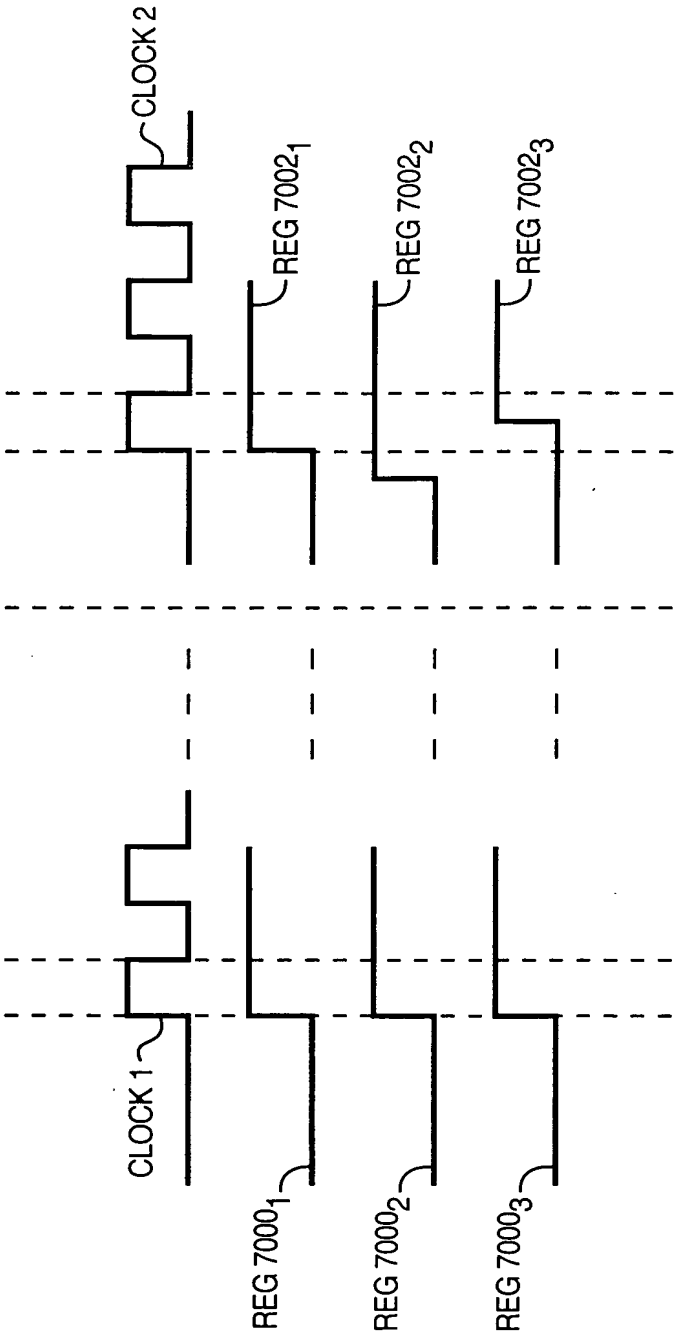

CLOCK 2
REG 7002$_1$
REG 7002$_2$
REG 7002$_3$
CLOCK 1
REG 7000$_1$
REG 7000$_2$
REG 7000$_3$

FIG. 19

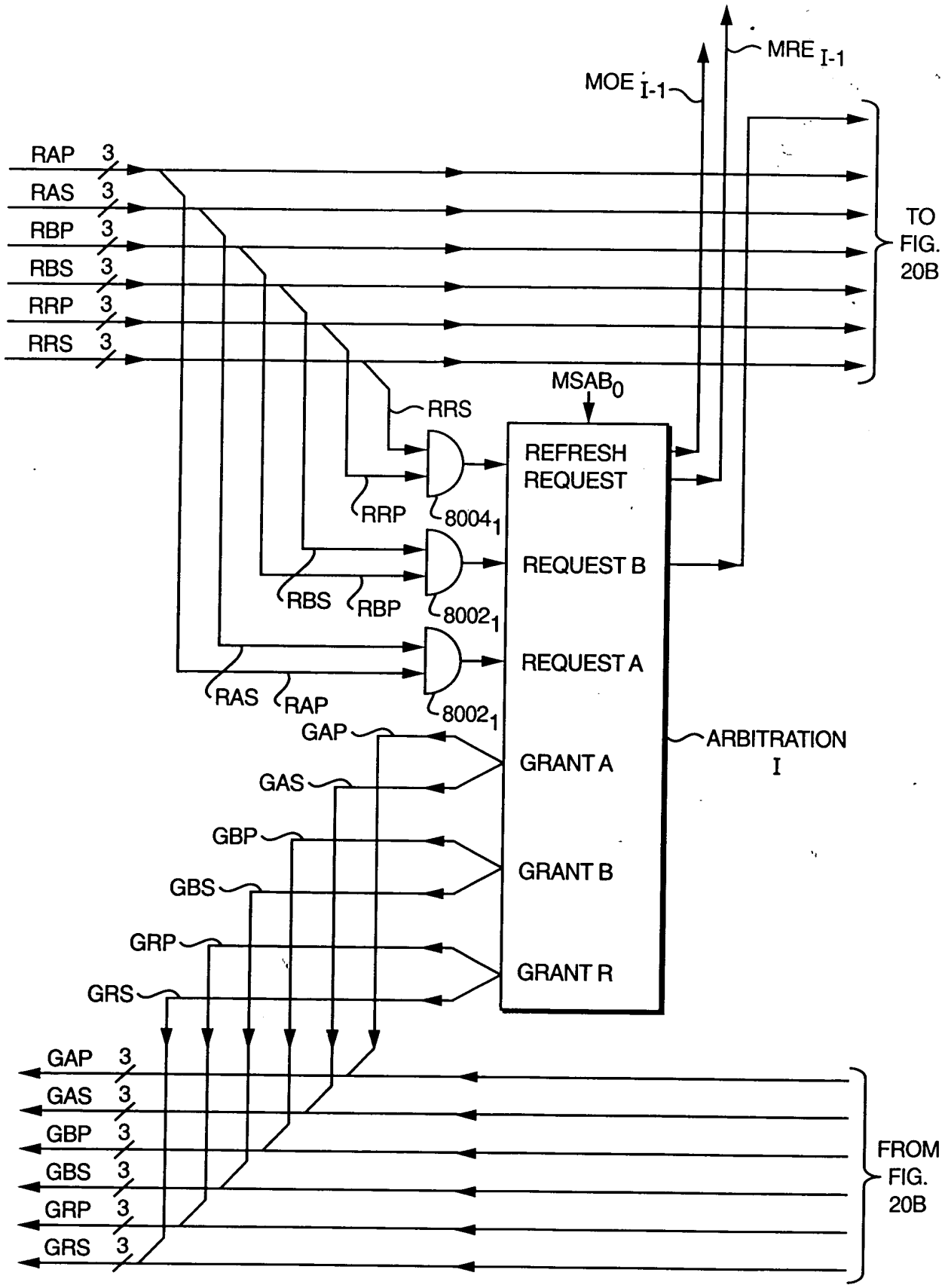

MRE I-1
MOE I-1
RAP 3
RAS 3
RBP 3
RBS 3
RRP 3
RRS 3
TO FIG. 20B
MSAB0
RRS
REFRESH REQUEST
RRP
8004 1
REQUEST B
RBS
RBP
8002 1
REQUEST A
RAS
RAP
8002 1
GAP
GAS
GRANT A
ARBITRATION I
GBP
GBS
GRANT B
GRP
GRS
GRANT R
GAP 3
GAS 3
GBP 3
GBS 3
GRP 3
GRS 3
FROM FIG. 20B

FIG. 20A

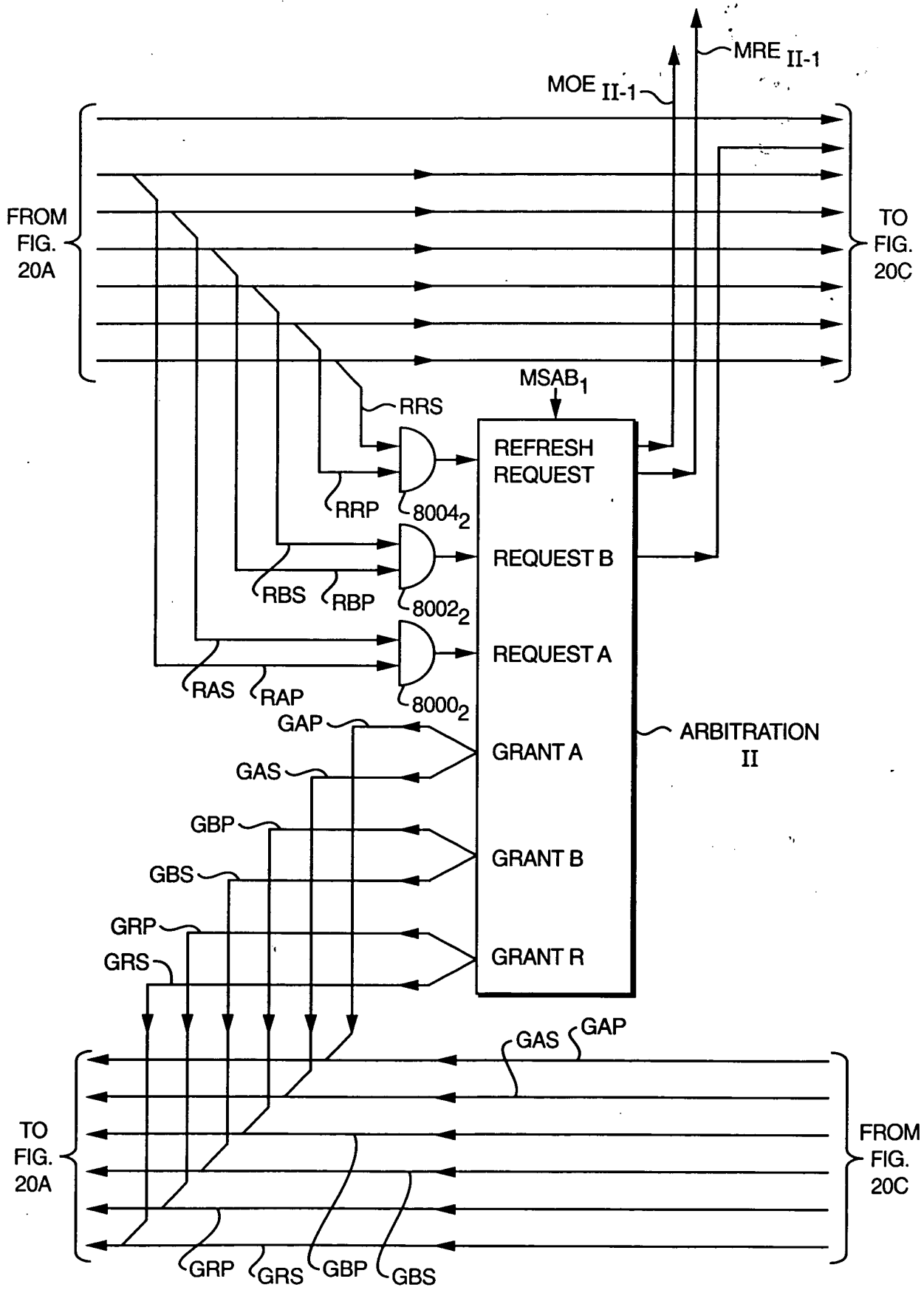

MRE II-1
MOE II-1
FROM FIG. 20A
TO FIG. 20C
MSAB1
RRS
RRP
8004 2
REFRESH REQUEST
REQUEST B
RBS
RBP
8002 2
REQUEST A
RAS
RAP
8000 2
GAP
GAS
GRANT A
ARBITRATION II
GBP
GBS
GRANT B
GRP
GRS
GRANT R
GAS
GAP
TO FIG. 20A
FROM FIG. 20C
GRP
GRS
GBP
GBS

FIG. 20B

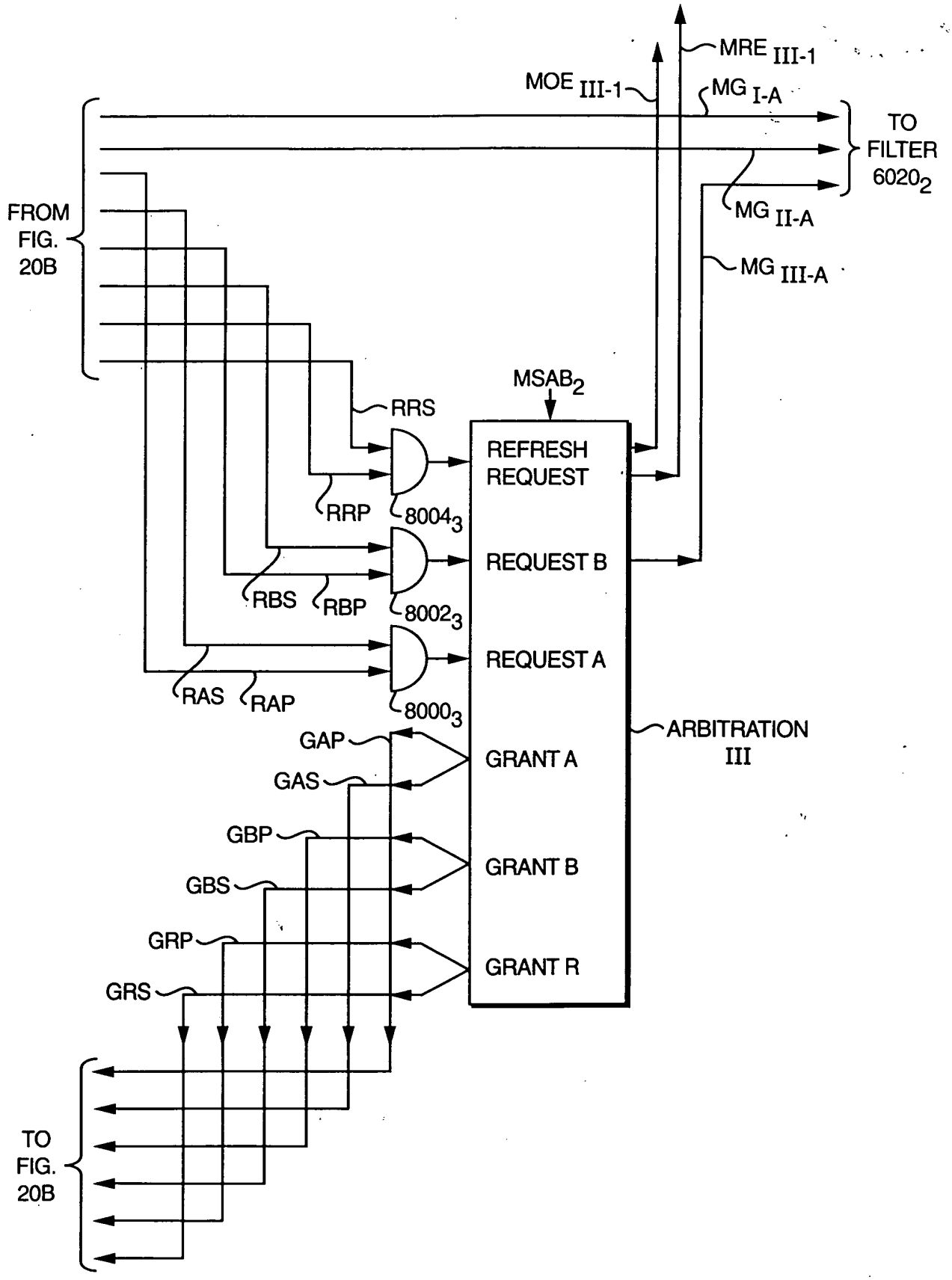

MRE III-1
MOE III-1
MG I-A
TO FILTER 6020$_2$
MG II-A
MG III-A
FROM FIG. 20B
MSAB$_2$
RRS
REFRESH REQUEST
RRP
8004$_3$
REQUEST B
RBS
RBP
8002$_3$
REQUEST A
RAS
RAP
8000$_3$
ARBITRATION III
GAP
GRANT A
GAS
GBP
GRANT B
GBS
GRP
GRANT R
GRS
TO FIG. 20B

FIG. 20C